"DESIGN OF ROBUST CLOCKING CIRCUIT FOR MODERATE SPEED VLSI CHIP APPLICATIONS"

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CERTIFICATE

This is to certify that the thesis entitled, ***"Design of Robust Clocking Circuit for Moderate Speed VLSI Chip Applications"*** submitted by ***Rupali Ashok Walunj*** is a bonafied work carried out by her, under the guidance of ***Prof. (Dr.) G. K. Kharate***, and it is approved for the partial fulfillment of the requirement of the Savitribai Phule Pune University, Pune, for the award of the degree of ***Doctor of Philosophy*** prescribed by Research Centre, ***Department of Electronics and Telecommunication Engineering***, ***Matoshri College of Engineering and Research Centre, Nashik-422105.*** She has fulfilled the requirements of the submission of the thesis. The material obtained from other sources has been duly acknowledged in the thesis. The results embodied in this thesis have not been submitted to any other institute or university for the award of any degree or diploma.

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Walunj Rupali Ashok

Abstract

Technology scaling has pushed power as a forefront design metric. Moreover, in recent years the design low power circuits have gained lot of attention due to increasing demand of portable electronics. Sub threshold operation quenches the Ultra-Low Power (ULP) demand of multitude of applications such as pace maker, RFID tags, biomedical sensors and wireless sensors but, at the cost of degraded performance and exacerbated variability. Low power consumption is an essential requirement for such applications since battery charging or replacement is infeasible. Clock circuit plays a very crucial role in communication sub systems like modulation, demodulation, frequency synthesizer, clock data recovery etc in these applications. Therefore design of ULP clock circuit has great potential to have prolonged battery life. This work focuses on design of ULP robust clock circuit for moderate speed applications.

The first part of this work investigates the bottlenecks in design of ULP clock circuit. The thesis reports that the clock system with un-buffered tree is a better option in sub threshold region compared to buffered tree. The results obtained in investigating the overall impact of variation in device and interconnect shows that device variation is dominant source in bringing about variability in clock system parameters. The performance of conventional CMOS based, DTMOS (Dynamic Threshold MOS) based and hybrid clock generator circuits are explored in this work. This work proposes a scheme to improve the thermal stability of ULP clock generator circuit. The proposed clock circuit produces stable clock frequency over a wide range of temperatures as compared to the conventional current starved voltage controlled oscillator (CSVCO) circuit with minimal increase in the power dissipation.

Further, this work investigates the suitability of conventional clock distribution network for sub threshold regime and proposes a novel strategy of having an optimized uniform H tree with a pair of buffer only at nodes where clocked element is connected in CDN. Furthermore, the viability of devices beyond CMOS such as Fin-FET and CNFET for sub threshold clock circuit is explored. Performance analysis of different configurations of CNFET and Fin-FET based clock circuit is accentuated in this work. The optimization of CNFET based clock circuit is done in order to have

better circuit performance. Finally, the performance comparison of CMOS VCO, DG Fin-FET based pignsg VCO and optimized CNFETVCO-3 is reported in this work. The result shows that that CNFET based optimized CNFETVCO-3 exhibits better performance in terms of energy efficiency as well as robustness.

List of Tables

Table No.	Illustration	Page No.
3.1	32 nm Berkeley Predictive Technology Model (PTM) device parameters	29
3.2	Default parameter values used for CNFET simulations	51
4.1	Comparison of proposed system with the published work	70
4.2	Comparison of performance parameters of DG FinFET based CSVCO configurations	79
4.3	Summary of performance and power consumption of DG FinFET CSVCO configurations	85
4.4	Summary of variability results of DG FinFET CSVCO configurations	86
4.5	Summary of proposed VCO with existing VCO in literature	86
4.6	Comparison of performance parameters of various CNFET CSVCO configurations	92
4.7	Performance parameters of various CNFET CSVCO configurations with varying control voltage	95
4.8	Summary of proposed VCO with existing VCO in literature	101

List of Figures

Figure No.	Illustration	Page No.
2.1	32nm NMOS drain current (I_D) versus gate to source voltage (V_{GS})	8
2.2	Schematic of a MOSFET with its capacitance components	10
2.3	Clock system	14
2.4	Typical clocked data path	14
2.5	Model of interconnect driven by driver in weak inversion region	18
3.1	The clock circuit with un-buffered H tree	27
3.2	The clock circuit with buffered H tree	27
3.3	Tapered H clock distribution network (design1)	28
3.4	RLC model for Cu interconnect	28
3.5	Tapered H clock distribution network (design2)	30
3.6	Schematic of CSVCO	32
3.7	Proposed control circuit to combat temperature variation effect	37
3.8	Proposed ULP voltage controlled ring oscillator with reduced temperature sensitivity	39
3.9	Impact of width variation on slew	40
3.10	Impact of spacing variation on slew	40
3.11	Impact of aspect ratio variation on slew	40
3.12	H tree with various configurations of buffers at sink nodes	41
3.13	Schematic of SG CSVCO	44

3.14	Schematic of IG CSVCO	44
3.15	Schematic of Hybrid CSVCO	45
3.16	Schematic of Hybrid reverse CSVCO	45
3.17	Schematic of pignsg CSVCO	45
3.18	Schematic of psgnig CSVCO	46
3.19	Schematic of MIGFET CSVCO	46
3.20	Drain current variation for change in gate to source voltage	49
3.21	Schematic of CNFETVCO-1	50
3.22	Schematic of CNFETVCO-2	50
3.23	Schematic of CNFETVCO-3	50
3.24	Schematic of CNFETVCO-4	51
4.1	Impact of voltage scaling on slew	53
4.2	Impact of voltage scaling on latency	54
4.3	Impact of voltage scaling on power	55
4.4	Impact of process variation and PVT variation on slew for buffered and un-buffered tree	55
4.5	Impact of process variation and PVT variation on latency for buffered and un-buffered tree	56
4.6	Impact of process variation and PVT variation on pulse width for buffered and un-buffered tree	56
4.7	Comparison of slew of buffered and un-buffered tree under nominal conditions and with W, T and S variation	57
4.8	Comparison of latency of buffered and un-buffered tree under nominal conditions and with W, T and S variation	58

4.9	Comparison of slew variation of buffered and un-buffered tree with PVT variation and PVT +interconnect variation in W, T and S	58
4.10	Comparison of latency variation of buffered and un buffered tree with PVT variation and PVT +interconnect variation in W,T and S	59
4.11	Comparison of slew for design1 and design2 for clock system with un-buffered tree	59
4.12	Comparison of slew for design1 and design2 for clock system with buffered tree	60
4.13	Comparison of latency for design1 and design2 for clock system with un-buffered tree	60
4.14	Comparison of latency for design1 and design2 for clock system with buffered tree	60
4.15	Comparison of slew variation for design1 and design2 for clock system with un-buffered tree	61
4.16	Comparison of latency variation for design1 and design2 for clock system with un- buffered tree	61
4.17	Time period comparison of CMOS CSVCO and DTCSVCO variants	62
4.18	Slew parameter comparison of CMOS CSVCO and DTCSVCO variants	62
4.19	PDP Comparison of CMOS CSVCO and DTCSVCO variants	63
4.20	Impact of process variation on time period of CMOS CSVCO and DTCSVCO variants.	63
4.21	Impact of temperature variation on time period of DTCSVCO-2 at different process corners and conventional CSVCO.	64
4.22	Time period versus temperature for conventional VCO at 0.9V (super threshold)	65
4.23	Time period versus temperature for conventional VCO at 0.3V supply voltage (sub threshold)	65

4.24	Variation in temperature coefficient of delay and power consumption at different supply voltages in sub threshold	66
4.25	Vtemp as a function of temperature	67
4.26	Control voltage as a function of temperature	67
4.27	Time period as a function of temperature	68
4.28	Clock pulse width variation with temperature for uncompensated VCO	68
4.29	Clock pulse width variation with temperature for compensated VCO	69
4.30	Power consumption of compensated and conventional sub threshold VCO	69
4.31	Slew of clock system with buffered and un-buffered tree	70
4.32	Comparison of tapered and optimized H tree slew performance	71
4.33	Performance comparison of optimized CDN with various configuration of buffer in last stage	72
4.34	Slew comparison of clock circuit with conventional tapered un-buffered CDN and with optimized uniform CDN with configuration3	72
4.35	Power consumption comparison of clock circuit with conventional tapered un- buffered CDN and with optimized uniform CDN with configuration3	73
4.36	Impact of temperature variation on slew and power for clock circuit with tapered un-buffered CDN	73
4.37	Impact of temperature variation on slew and power for clock circuit with proposed CDN	74
4.38	Impact of process variation on slew for clock circuit with tapered un-buffered CDN	74
4.39	Impact of process variation on slew for clock circuit with proposed CDN	74

4.40	Slew as a function of temperature at different process corners	75
4.41	Performance Comparison of CMOS and Hybrid clock system	76
4.42	PDP comparison of Bulk CMOS and DG FinFET CSVCO with variation in supply voltage	76
4.43	EDP comparison of Bulk CMOS and DG FinFET CSVCO with variation in supply voltage	77
4.44	PDF for Bulk CMOS CSVCO	77
4.45	PDF for DG FinFET CSVCO	78
4.46	PDF for Bulk CMOS CSVCO	78
4.47	PDF for Bulk DG FinFET	78
4.48	Variation of pulse width of DG FinFET CSVCO variants with oxide thickness for sub threshold operation	80
4.49	Variation of PDP of DG FinFET CSVCO variants with oxide thickness for sub threshold operation	80
4.50	EDP variation sensitivity of DG FinFET CSVCO variants with oxide thickness for sub threshold operation	81
4.51	The pulse width variation sensitivity of DG FinFET CSVCO variants with tsi for sub threshold operation	81
4.52	Variation of PDP of DG FinFET CSVCO variants with tsi for sub threshold operation	82
4.53	EDP variation sensitivity of DG FinFET CSVCO variants with tsi for sub threshold operation	82
4.54	Variation of pulse width of DG FinFET CSVCO variants with supply voltage for sub threshold operation	83
4.55	Variation of PDP of DG FinFET CSVCO variants with supply voltage for sub threshold operation	83

4.56	EDP variation sensitivity of DG FinFET CSVCO variants with supply voltage variation for sub threshold operation	84
4.57	Variation of pulse width of DG FinFET CSVCO variants with temperature for sub threshold operation	84
4.58	Variation of PDP of DG FinFET CSVCO variants with temperature for sub threshold operation	84
4.59	EDP variation sensitivity of DG FinFET CSVCO variants with temperature variation for sub threshold operation	85
4.60	Tuning characteristics of CMOS and CNFET based VCO	87
4.61	Drain current variation for change in gate to source voltage for 32nm N type MOSFET and 32nm NCNFET	88
4.62	Variation in power with variation in control voltage	89
4.63	PDP comparison of Bulk CMOS and CNFET CSVCO with variation in supply voltage	89
4.64	EDP comparison of Bulk CMOS and CNFET CSVCO with variation in supply voltage	90
4.65	PDF for Bulk CMOS CSVCO	90
4.66	PDF for CNFET CSVCO	91
4.67	PDF for Bulk CMOS CSVCO	91
4.68	PDF for CNFET CSVCO	91
4.69	Variation of Pulse Width of CNFETVCO variants with supply voltage for sub threshold operation	93
4.70	Variation of PDP of CNFETVCO variants with supply voltage for sub threshold operation	93
4.71	EDP variation of CNFETVCO variants with supply voltage variation for sub threshold operation	93
4.72	Frequency variation with control voltage variation	94

4.73	Power variation with control voltage variation	94
4.74	Variation of PDP of CNFETVCO variants with variation in temperature for sub threshold operation	95
4.75	Variation of pulse width of CNFETVCO variants with variation in chirality vector	96
4.76	Variation of PDP of CNFETVCO variants with variation in chirality vector	96
4.77	Variation of EDP of CNFETVCO variants with variation in chirality vector	96
4.78	Pulse Width and PDP as a function of number of tubes of CNFETs in current sources and sinks	97
4.79	Pulse Width and PDP as a function of pitch for tubes in CNFETs of current sources and sinks	98
4.80	Pulse Width and PDP as a function of diameter of tubes of all CNFETs	98
4.81	Pulse Width and PDP as a function of oxide thickness	99
4.82	Performance comparisons of various CNFETVCO configurations 1-CNFETVCO-1, 2-CNFETVCO-2, 3-CNFETVCO-3, 4-CNFETVCO-4, 5-Optimized CNFETVCO-3	99
4.83	Tuning characteristics of CNFETVCO -3 and optimized CNFETVCO-3	100
4.84	Variation in power with variation in control voltage	100
4.85	PDF for CNFETVCO variants	101
4.86	PDP comparison of CMOS, DG FINFET pignsg and Optimized CNFETVCO-3	102
4.87	EDP comparison of CMOS , DG FINFET pignsg and Optimized CNFETVCO-3	102
4.88	PDF for CMOS CSVCO	103

4.89	PDF for DG FinFET pignsg VCO	103
4.90	PDF for Optimized CNFETVCO-3	104
4.91	PDF for CMOS CSVCO	104
4.92	PDF for DG FinFET pignsg VCO	104
4.93	PDF for Optimized CNFETVCO-3	105

List of Symbols

Symbol	Illustration
n, m	Chiral vector
a	Lattice constant
C_{dep}	Depletion capacitance
C_g	Gate capacitance
C_L	Load capacitance
C_{if} and C_{of}	Input and output fringe capacitance
Cox	Gate oxide capacitance
D_{CNT}	Diameter of a CNT
E_g	Energy gap
gm	Tran conductance
I_D	Sub threshold drive current
I_{OFF}	Transistor off current
I_{ON}	Transistor on current
k_B	Boltzmann's constant
L_{eff}	Effective Channel Length
N_{eff}	Effective Channel Doping
S	Sub threshold Slope
T_d	Gate delay

T_{ox}	Oxide thickness
t_r	Rise time
t_{su}	Set up time
t_{hold}	Hold time
V_{DD}	Supply voltage
n	Body effect coefficient
Φ_s	Surface potential
Φ_F	Fermi potential
Vtho	Zero bias threshold voltage
η	DIBL effect coefficient
μ	mobility
ε_{si}	Relative permittivity of silicon
α	Activity factor
g_{CNT}	Transconductance per CNT

List of Abbreviations

AR	Aspect Ratio
CDN	Clock Distribution Network
CNT	Carbon Nanotube
CNFET	Carbon Nanotube Field Effect Transistor
CNFETVCO	CNFET based VCO
CSVCO	Current Starved Voltage Controlled Oscillator
Cu	Copper
DG Fin-FET	Double Gate Fin-FET
DIBL	Drain Induced Barrier Lowering
DTMOS	Dynamic Threshold MOS
DTCSVCO	DTMOS based CSVCO
EDP	Energy Delay Product
IG	Independent Gate
ITRS	International Technology Roadmap For Semiconductor
MIGFET	Multiple Independent Gate Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PDF	Probability Density Function
PDP	Power Delay Product
PPM	Parts Per Million

PVT	Process, Voltage and Temperature
RDF	Random Dopant Fluctuations
R_{driver}	Driver resistance
SG	Short Gate
SLP	Slew-Latency Product
SRAM	Static Random Access Memory
RO	Ring Oscillator
ULP	Ultra Low Power
VCO	Voltage Controlled Oscillator
$V_{control}$	Control Voltage
V_{DD}	Supply Voltage
VLSI	Very Large Scale Integration
V_{th}	Threshold Voltage
V_{tho}	Zero Bias Threshold Voltage
V_T	Volt Equivalent of Temperature
V_{bs}	Bulk Source Voltage

Chapter 1

INTRODUCTION

1.1 Overview

In today's era of portable electronics, power consumption has emerged as an important design metric. Intended sub threshold circuits have proven their ability to satisfy the demand of Ultra Low Power (ULP) consumption of multitude of applications such as pace makers, hearing aids, RFID tags, wireless sensors etc. but, at the cost of degraded performance and exacerbated variability. Low power consumption is an essential requirement for such applications since, battery charging or replacement is difficult. These ULP applications have very stringent space and low power constraints with moderate speed requirement. Clock circuit plays a very crucial role in communication and signal processing subsystems in these applications. Moreover, clock circuit significantly affects performance and power consumption of a system. Therefore, efforts taken to design the ULP clock circuit will eventually reduce the overall power consumption of these applications. Though, sub threshold circuits are the best alternative to achieve low power, the major challenge in working in this region is to reap the advantage of ULP benefits with minimal degradation of speed & robustness. Hence, there is a need to address the speed and robustness issues of ultra low power clock circuit. This work explores the different techniques to improve performance and robustness of clock circuit under sub threshold conditions for moderate speed VLSI chip applications.

1.2 Motivation

Clock circuit is an inevitable part of synchronous digital system. Moreover, clock circuit plays a vital role in governing the reliability, power consumption and performance of synchronous system. Although the numbers vary from design to design, VLSI circuit like FPGA typically dissipate 60%–70% of their power in the interconnect network, 10%–20% in the clock network, and 5%–20% in logic [1]. Therefore there is a pressing need to focus on design of clocking circuits for applications having stringent power budget [1]. Moreover, in the ubiquitous era of ULP applications such as wireless sensor nodes, pace makers, RFID tags etc power consumption is of primary concern. Clock circuit is a vital component in these

applications. Low power, low area and simple implementation are the key features required by a clock circuit in order to be incorporated in implantable biomedical systems or sensor networks. Minimizing the supply voltage (V_{DD}) is the most popular method to achieve low power since dynamic power consumption is quadratic function of V_{DD} whereas static power is its exponential function [2]. The extreme case of V_{DD} reduction is to reduce it below threshold voltage called as sub threshold operation [3]. Since sub threshold circuits have huge potential to satisfy the ULP demand, design of clock circuit in sub threshold regime will reduce the overall power consumption of the power sensitive applications.

Though the sub threshold operation is a promising approach to satisfy the ULP demand but, degraded performance and increased variability are its major limitations as reported by the researchers. The literature review in this work reveals that though the researchers have proposed different techniques at device and interconnects level to improve the performance and mitigate the variability issues in sub-threshold regime, very few researchers have worked on developing the clocking strategies for circuits working under sub-threshold conditions.

Therefore, there is a pressing need to focus on design of sub threshold clock circuits. Degraded performance and variability are the stumbling blocks that provide hindrance to the wide applicability of sub threshold circuits. Therefore, motivated by these factors this research work focuses on design of robust clock circuit in sub threshold regime.

1.3 Problem Statement and Objectives

- **Problem Statement**

The primary goal of this research work is to design an integrated Ultra Low Power and PVT (Process, Voltage and Temperature) insensitive clocking circuit for moderate speed VLSI chip applications.

- **Objectives**

1 To understand the low power interconnects techniques, clock generation and distribution circuits for ultra low power applications.

2 To review the research literature to understand the various challenges in design of clock generation and distribution circuit for low power applications and interconnect techniques for sub threshold circuits.

3 To design a robust clock circuit for sub threshold applications at suitable biasing using bulk CMOS and devices beyond CMOS; FinFET, CNFET.

4 To optimize the various parameters of clock circuit for portable applications having stringent power budget.

5 To develop the proposed designed clock circuit using suitable tools and verify the results.

6 To validate the results of proposed work.

1.4 Research Contributions

Following are the key contributions made by the research work while designing robust clock circuit for ULP applications.

- This work investigates the impact of voltage scaling on performance parameters of clock circuit with buffered as well as un-buffered Clock Distribution Network (CDN). The findings in this work shows that, the device variations are of primary concern whereas the interconnect variations are of secondary importance in bringing about variability in well designed parameters of clock system in sub threshold regime. Furthermore, the variability analysis explored in this work indicates that the clock generator is major source of jitter.
- This work investigates the performance of buffered and un-buffered CDN and proposes clock system with un-buffered tree in sub threshold regime. Furthermore, an attempt to improve slew of the sub threshold un-buffered CDN is made in this work by redesigning the H tree CDN.
- The performance of conventional CMOS based, Dynamic Threshold MOS (DTMOS) based and hybrid (combination of MOS and DTMOS) clock generator circuits are explored in this work. The results indicate that the proposed hybrid DTCSVCO-2 clock generator proves to be energy efficient and exhibits better performance in terms of switching speed as well as robustness compared to conventional CMOS Current Starved Voltage Controlled Oscillator (CSVCO).
- A scheme to improve the thermal stability of the sub threshold clock generator is accentuated in this work. A combination of temperature monitoring circuit and control circuit has been designed and incorporated to develop a thermally robust clock generator. A novel control strategy is developed, wherein the control voltage is adaptively altered to combat the exponential change in the clock period

with the variation in temperature, without use of any passive components like resistors and capacitors. The proposed ULP clock generator produces stable clock frequency over a wide range of temperature.

- A novel strategy of having an optimized H tree with a pair of buffer, only at the point of contact of CDN with clocked element, is proposed in this work. The performance of various configuration in which the pair of buffer can be connected in CDN is investigated. Finally, the optimized uniform H tree with CMOS buffer connected to clocked element followed by dynamic threshold MOS (DTMOS) buffer is proposed in this work. The proposed strategy shows improvement in slew with added advantage of reduced power consumption and robustness as compared to conventional CDN.
- Furthermore, this work investigates the viability of DG FinFET clock generator in the sub threshold regime. Seven different CSVCO configurations viz. SG, IG, hybrid, hybrid reverse, pignsg, psgnig and MIGFET CSVCO are designed and analyzed in this work. The proposed pignsg CSVCO exhibits better performance and robustness compared to the other configurations.
- Carbon Nano Tube Field Effect Transistor (CNFET) technology is a promising alternative to the CMOS technology. This work investigates the viability of CNFET CSVCO by comparing the performance of CMOS based and CNFET based CSVCO. Furthermore, four CNFET based CSVCO configurations viz. CNFETVCO-1, CNFETVCO-2, CNFETVCO-3 and CNFETVCO-4 are designed at 32 nm technology node using Stanford CNFET model and analyzed in this work. The proposed CNFETVCO-3 exhibits better results compared to other CSVCO configurations in terms of performance and robustness. Furthermore, CNFETVCO-3 is optimized by selecting the optimal number of tubes, pitch, CNT diameter and oxide thickness to achieve better speed to further improve the performance and robustness.
- This work highlights the performance and robustness comparison of CMOS based, DG FinFET based pignsg and CNFET based optimized CNFETVCO-3 CSVCO. Performance of optimized CNFETVCO-3 circuit is greatly improved in terms of speed as well energy efficiency compared to pignsg and CMOS based CSVCO. The spread in pulse width for optimized CNFETVCO-3 is reduced compared to other two VCO thus exhibiting better robustness.

1.5 Organization of Thesis

This research work targets towards designing a robust ULP clock circuit for sub threshold applications. The structure of this thesis is as follows:

- Chapter 1 gives the introduction of design of low power clock circuit. It discusses about the motivation and objectives and briefs the contributions of this work.
- Chapter 2 overviews the different sources of power consumption in nano-scale CMOS technology. Further, this chapter reviews the work done at device and interconnects level in sub threshold regime. The clock system basics are also accentuated in this chapter. This chapter also reviews related research work in design of low power clock circuit.
- Chapter 3 deals with the design of various schematics of clock generator circuits with CMOS and devices beyond CMOS. A scheme to improve the thermal stability of the sub threshold VCO is presented in this chapter. It also presents the design of slew aware ULP CDN.
- Chapter 4 reports and discusses the simulation results obtained by simulating various schematics of clock circuits.
- Chapter 5 includes the conclusions of the thesis and suggests the direction for future work.

Chapter 2

LITERATURE SURVEY

Semiconductor industry has proliferated and made a rapid growth in many diversified applications which encompasses health care, education, security and communications. Technology scaling has been the primary driving force for technological advancements. In order to increase the performance & component density, devices have been miniaturized with tremendous speed. Though, the technology scaling has increased the performance, it has also increased the power density substantially. Moreover, technology scaling has pushed power at forefront and hence, power has emerged as an important design parameter. Also, in recent years portable applications have attracted the semiconductor industry and compelled for ULP circuit design. This chapter reviews the sources of power dissipation. It also focuses on power efficient sub threshold operating region followed by discussion on clock system basics and review of low power clock circuits.

2.1 Power Dissipation in VLSI Circuits

The enhancement in device performance and maximum number of devices on a chip by evolutionary device scaling and/or increased chip size has increased the power dissipation. Therefore, to minimize the adverse effects of increased self heating problems and to extend the battery life, power has emerged as an important design parameter and has received considerable attention in recent years. The total power dissipation in CMOS circuits consists of two main components; dynamic and static power dissipation.

- **Dynamic power dissipation:**

Dynamic power dissipation has two components; switching power and short circuit power [4]. Charging and discharging of load capacitance constitutes switching power and non-zero rise and fall times leads to short circuit power. The switching power of a single gate is given by equation 2.1[4].

$$P_{dyn} = \alpha f C_L V_{DD}^2 \qquad \text{.....2.1}$$

where, f is the clock frequency, C_L is load capacitance, V_{DD} is the supply voltage and

α is the activity factor.

During switching of input, both pull up and pull down networks are partially on for a short duration. This provides a direct path between supply and ground leading to short circuit power dissipation. The short circuit power is given by equation 2.2 [5].

$$P_{sc} = \frac{\beta}{12}\left(V_{DD} - V_{th}\right)^3 \frac{\tau}{T} \qquad \text{.....2.2}$$

where, β is the transistor coefficient, τ is rise/fall time, V_{th} is the threshold voltage and T is the time delay.

- **Static power dissipation:**

The static power dissipation is due to leakage current as indicated by equation 2.3.

$$P_{static} = I_{leakage} V_{DD} \qquad \text{.....2.3}$$

The static power component is due to static conductive paths between supply rails, even when there is no switching. It is well established that even though continuous technology scaling is able to reduce the active power, static leakage power increases significantly and may exceed the active power for future technologies [6]. The nanometre processes with low threshold voltage, thin gate oxide and halo doping accounts to increase in static power dissipation.

2.2 Sub threshold Operation

Extensive research has been reported by the researchers in order to reduce the dynamic as well as static power to have low power VLSI chips. V_{DD} scaling, switching activity reduction, device sizing, and interconnect optimization techniques are various methods proposed by the researchers to reduce the power consumption [2]. V_{DD} scaling reduces dynamic power quadratically as indicated by equation 2.1 Moreover, V_{DD} scaling also reduces static power as shown by equation 2.3. Therefore, V_{DD} scaling is most successful method for power reduction.

Nevertheless, for energy constrained VLSI applications such as pace makers, hearing aids, RFID tags, biomedical and wireless sensors, ULP consumption is the major parameter for the design considerations. Therefore, ULP energy efficient design technique has been grown considerably in recent years [7, 8]. Operating the transistors in digital logic at the sub-threshold region has been proposed by the researchers to achieve ULP [3]. Operating the device in sub-threshold region, where $V_{DD} < V_{th}$, can

achieve the lower power consumption as compared to conventional super-threshold operation due to lower V_{DD} and smaller gate capacitance [9]. Moreover, Short Channel Effects (SCEs) like Drain Induced Barrier Lowering (DIBL), quantum mechanical gate tunnelling, and punch through are eliminated in sub-threshold region of operation. Due to exponential V-I characteristics in the sub-threshold region, the devices have a high trans-conductance gain.

2.2.1 Sub threshold Circuit Performance Metrics

The performance metrics for sub threshold circuit design are sub threshold current, ON–OFF current ratio, sub threshold slope (S), gate capacitance (C_g), gate delay (T_d), Power Delay Product (PDP) and Energy Delay Product (EDP).

- **Sub threshold Current**

The sub threshold current is the current which flows between the source and drain of a MOSFET when the transistor is in sub threshold region. The sub threshold leakage current, given by equation 2.4, acts as the driving current in sub threshold operation in bulk CMOS [10],

$$I_D = I_0 e^{\frac{(V_{GS}-V_{th})}{nV_T}} \qquad \text{.....2.4}$$

Where, V_{GS} is the gate to source voltage, V_{th} is the threshold voltage, I_0 is the current that flows when $V_{GS}=V_{th}$, V_T is the thermal voltage, The slope factor 'n' in exponential term represents the effect of the capacitive divider formed by the oxide capacitance C_{OX} and the depletion capacitance C_d.

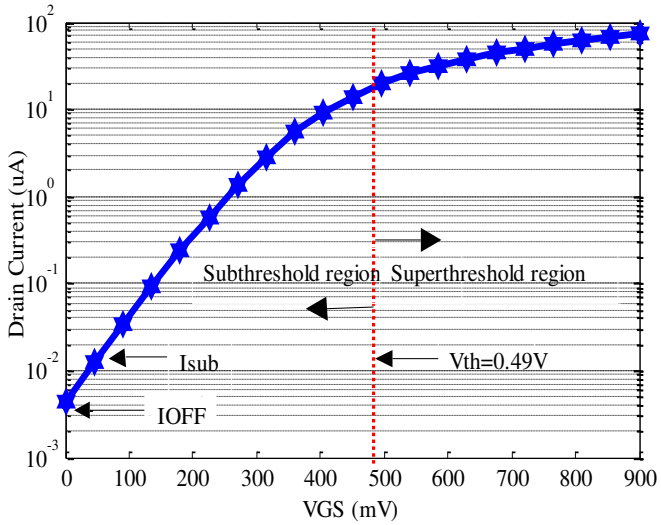


Figure 2.1: 32nm NMOS drain current (I_D) versus gate to source voltage (V_{GS})

In sub threshold region, also referred as the weak inversion region, drain current is exponentially dependent on V_{th} and V_{GS} as shown in Figure 2.1.

- **ON–OFF Current Ratio (I_{ON}/I_{OFF})**

It is a ratio of sub-threshold current, I_{ON} at $V_{GS}=V_{DS}=V_{DD}$ and sub threshold current, I_{OFF} at $V_{GS}=0$ and $V_{DS}=V_{DD}$ for $V_{DD}<V_{th}$. Higher ON-OFF current ratio gives better performance as well as robustness.

- **Sub threshold Slope (S)**

Sub threshold slope is a parameter that determines the relationship between sub threshold current and the gate voltage. It is defined as inverse slope of the log (I_D) versus V_{GS} characteristics in sub threshold region. Sub threshold slope is the amount of gate to source voltage required to change the sub threshold current by an order of magnitude. It can be expressed by equation 2.5 [11].

$$S = 2.3V_T n \qquad \text{.....2.5}$$

$$S = 2.3V_T\left[1+\frac{3T_{OX}}{W_{dep}}\right]\left[1+\frac{11T_{OX}}{W_{dep}}e^{\left[\frac{-\pi L_{eff}}{2(W_{dep}+3T_{OX})}\right]}\right] \qquad \text{.....2.6}$$

where, $w_{dep} \propto \frac{1}{\sqrt{N_{eff}}}$ is the depletion width with an effective channel doping N_{eff}, V_T is thermal voltage, n is the sub threshold slope factor, L_{eff} is the effective channel length, and T_{OX} is the oxide thickness.

The value of sub threshold slope which is theoretically limited to values larger than 60mV/decade at T = 300 K, should be as small as possible to ensure the steepest sub-threshold characteristic. As indicated by equation 2.6, as L_{eff} of MOSFET decreases due to short channel effects in deep nanometer regime, sub threshold slope increases correspondingly.

- **Gate Capacitance (Cg) in Sub threshold**

Figure 2.2 shows the schematic of a MOSFET with its capacitance components (intrinsic and parasitic). Unlike super threshold region where input capacitance is dominated by the oxide capacitance, the input capacitance in sub threshold region is given by equation 2.7 [11].

$$C_g = \text{series}(C_{OX}, C_{dep}) \mid C_{if} \mid C_{of} \mid C_o \qquad \text{.....2.7}$$

\

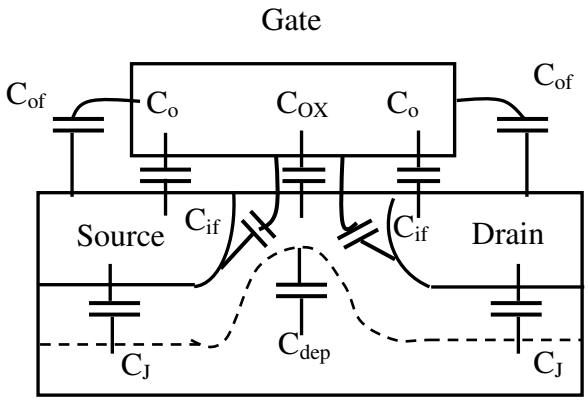


Figure 2.2: Schematic of a MOSFET with its capacitance components

Thus, input gate capacitance C_g in sub threshold regime is combination of intrinsic [oxide capacitance (C_{OX}) and depletion capacitance (C_{dep})] and parasitic [overlap capacitance (C_o), fringing capacitance (C_{if}, C_{of}) capacitances of a transistor as given by 2.7 [11]. Due to lower V_{DD} in the sub threshold region, the inversion charge is negligible. Therefore, the intrinsic capacitance is negligible. Thus, due to smaller capacitance and lower V_{DD}, sub threshold circuits consume less power compared to the conventional super threshold circuits.

- **Gate delay (T_d)**

The delay of a CMOS gate is given by equation 2.8 [8].

$$T_d = \frac{C_L V_{DD}}{I_{ON}} \qquad \text{…….2.8}$$

where, C_L is the load capacitance.

Gate delay can also be expressed in terms of sub threshold slope as given by equation 2.9 [12].

$$T_d \propto \frac{C_L S}{I_{OFF}} \qquad \text{…….2.9}$$

- **Power Delay Product (PDP) and Energy Delay Product (EDP)**

Power Delay Product (PDP) is a product of power and delay and is a measure to determine the energy efficiency of circuit. Power-Delay tradeoff is an important concern for circuit designers. The higher speed comes at the expense of higher power consumption. Decrease in power at the expense of large increase in delay is not an attractive option.

Energy Delay Product (EDP) is a metric that is more biased to performance. It balances energy as well as delay. Lower PDP and EDP imply better metrics for a system [13]. Minimum energy point occurs in sub threshold region.

2.3 Effect of Process, Voltage and Temperature (PVT) Variation in Sub threshold Regime

Variability is an important concern at deep nanometer technology nodes. The exponential dependency of sub threshold drive current on threshold voltage and temperature in sub threshold operating region further magnifies the impact of PVT variations.

Random dopant fluctuation (RDF) is a dominant source of variation in sub threshold region [14]. RDF causes variation in threshold voltage. Moreover, the consideration of threshold voltage (V_{th}) variability is utmost important since the process parameter like oxide thickness, channel length and channel doping have direct impact on V_{th}.

In strong inversion region, mobility dominates whereas in sub threshold region threshold voltage dominates. Therefore, increase in temperature leads to slower circuits in super threshold region whereas increases the speed of sub threshold circuits exponentially.

2.4 Review of Circuits Operated under Sub threshold Conditions

Though sub threshold operation of device can achieve orders of magnitude lower power consumption as compared to conventional super-threshold operation, the two important challenges in sub-threshold region of operation are its degradation in performance and increased sensitivity to PVT variations which is more pronounced due to exponential I–V characteristics [15]. Variability has direct impact on circuit delay, energy consumption and reliability.

Researchers have analyzed variability and degraded performance issues in sub-threshold regime and have suggested techniques to mitigate these issues. Upsizing of channel length considerably improves the sub-threshold swing, DIBL, and variability, leading to an important energy gain as suggested by the researchers in [16]. Tajalli and Leblebici proclaimed that the advantages of technology scaling in regard with energy consumption starts to decline for 45/32 nm technology nodes and below [17]. Further, these researchers experimentally and analytically showed that scaling V_{DD} in

deep sub-threshold region increases energy consumption and also investigated that optimum V_{DD} for minimum energy consumption lies in moderate sub-threshold region [17]. The effect of temperature variability on energy consumption for different V_{DD} and device sizes was explored by the researchers [18]. Also, the thermal impact on sub-threshold interconnects for different buffer-sizes and wire-lengths were studied. Researchers recommended the use of body bias technique to increase the robustness in sub-threshold circuits [19, 20]. When energy efficiency is a key performance criterion, use of dynamic frequency scaling was suggested by the researchers [21]. Researchers have demonstrated that performance of the digital circuits can be enhanced to a great extent by working in near threshold region [22]. The variability issue was addressed through device sizing and increased value of V_{DD} by the researchers in [14]. Adaptive power supply and body bias technique was used by the researchers in [23] to design a system which automatically took care of variations. Researchers claimed that the novel devices like FinFET promises to reduce threshold voltage variations and therefore can prove to be useful in mitigating variability [24]. Researchers have reported that the Si MOSFET device is optimized for super threshold region and have suggested that redesigning and optimizing the Si device for sub-threshold regime will surely enhance its performance and its applicability in low power application spectrum of VLSI [25]. The frequency of sub-threshold circuit can be enhanced by selecting optimum PMOS to NMOS width ratio [26].

Thus, researchers have investigated and suggested various techniques like body biasing, device sizing, redesigning and optimizing the Si device, near sub-threshold operation, alternative novel devices, upsizing the device to overcome the challenges in sub-threshold regime. Along with device, interconnect also plays a dominant role in enhancing the system's performance. With technology scaling, the global interconnects are becoming more resistive leading to larger delays. Therefore, there is a need to review the techniques suggested by the researchers to enhance the performance of interconnects from various perspectives.

Carbon Nano Tube (CNT) has been proposed as an attractive alternative to Cu wire interconnect in the deep submicron region for super threshold applications [27]. The applicability of conventional techniques to sub-threshold domain is investigated by the researchers. Conventionally, one of the popular design strategies is to reduce the

delay by buffer insertion technique which gives better performance by providing sharper slew and minimizing skew [28]. S. Pable and Mohd Hasan suggested that, since the driver delay dominates the interconnect delay under sub-threshold condition, repeater insertion in long line interconnect will further increase the delay as well as switching energy contrary to the super threshold region and hence, optimization of driver is essential in sub-threshold regime [29]. Also researchers in [30] reported that adding buffers cannot reduce delay. Thus, the benefits achieved in conventional super threshold regime may no longer withstand in sub-threshold.

The propagation delay for RC Cu interconnects driven by CMOS driver is given by equation 2.10 [31].

$$\Gamma_d = R_{driv}(C_{driv} + C_{load}) + 0.4R_W.C_W l^2 + (R_{driv}.C_W + R_W.C_{load})l \qquad \ldots\ldots.2.10$$

where, R_{driv} and C_{driv} are the driver resistance and capacitance respectively, R_w and C_w are interconnects resistance and capacitance, 'l' is the length of the wire and C_{load} is the load capacitance.

PVT variation exponentially changes the delay of buffers and hence makes buffer insertion inadequate for sub-threshold regime. Hence, repeater insertion is not beneficial under sub-threshold condition [30].

Researchers have explored the performance of interconnects in sub-threshold domain and accordingly suggested the methodologies to enhance their performance. J. Kil et al. in [32] explored gate voltage boosting technique to improve the sub-threshold interconnect performance and robustness. The researchers have concluded that in contrast to super threshold, repeater insertion in global interconnect will further increase the delay as well as switching energy [33]. Researchers have suggested to explore new aspect ratios of interconnect to reduce the interconnect capacitance for improving the performance in terms of delay and energy [29]. O. Jamal and A. Naeemi proposed CNT as interconnect instead of Cu, under sub-threshold conditions with V_{DD} of 100 mV at deep nanometer technology node (22/16/14 nm) [34]. The repeater insertion technique can only enhance the slew and it has adverse effect on interconnect delay as explored by researchers in [35].

Thus, significant research work has been carried out in sub-threshold. Though researchers have proposed different techniques at device and interconnect level to improve the performance and mitigate the variability issues in sub-threshold regime,

very few researchers have worked on developing the clocking strategies in sub threshold regime. Clock circuit plays a very crucial role in communication subsystems like modulation, demodulation, frequency synthesizer, clock data recovery and is an inevitable block in many systems. The next section describes the basics of clock system and reviews the previous work in designing the clock circuit.

2.5 Clock System

A clock system generates and distributes the clock signal. This signal does an important job of ordering multitude of events in a system by providing the temporal reference for the movement of data. It governs the pace of data transfer and hence performance of system. In order to ensure the reliable operation of a synchronous system, certain timing constraints are imposed on the clock system design metrics. Non compliance of these restrictions often leads to functional failure, thus questioning the reliability of system. Also, since clock signal has highest switching activity, Clock Distribution Network (CDN) in clock system consumes about 40% of total dynamic power [36].

2.5.1 Timing Basics of Synchronous System

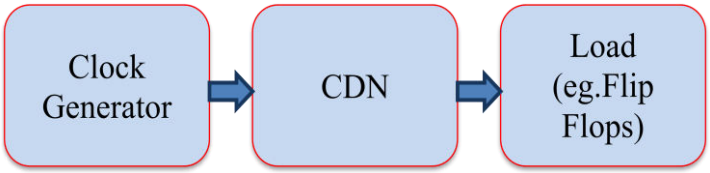


Figure 2.3: Clock system

Figure 2.3 shows a clock system. Clock generator and Clock Distribution Network (CDN) together constitute a clock system. Clock generator shoulders the responsibility of generating clock signals, whereas these clock signals are disseminated throughout the chip to the clocked elements via CDN.

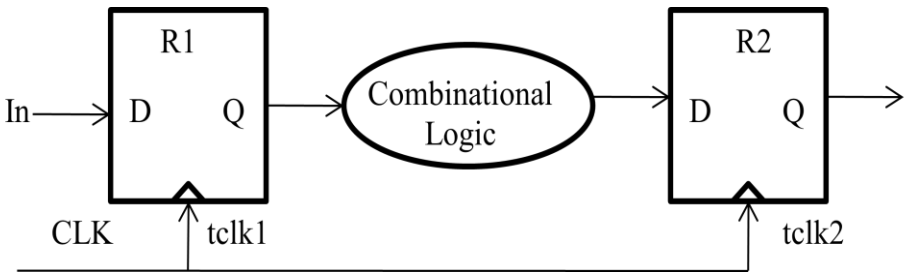


Figure 2.4: Typical clocked data path

As shown in Figure 2.4, a typical synchronous data path is a network of clocked elements and combinational logic [4]. Ideally clock signal reaches to all the clocked elements simultaneously. Under ideal conditions, the maximum clock period of a system is given by equation 2.11 [4].

$$t_{clk} > t_{c\text{-}q} + t_{logic} + t_{su} \quad \text{.....2.11}$$

where, t_{clk} is the clock period, $t_{c\text{-}q}$ refers to propagation delay of register, t_{logic} refers to propagation delay of combinational logic, t_{su} is the set up time for the registers.

Along with above constraint, to avoid the races, the hold time of register must also satisfy the condition given in equation 2.12,

$$t_{hold} < t_{c\text{-}q,cd} + t_{logic,cd} \quad \text{.....2.12}$$

where, t_{hold} is the hold time for the registers, $t_{c\text{-}q,cd}$ and $t_{logic,cd}$ are minimum propagation delay of register and logic respectively.

But, unfortunately the ideal condition never exists and there are certain clock uncertainties with clock signal having both temporal and spatial variations referred to as clock jitter and skew respectively. These uncertainties in clock signal further imposes the timing constraint on minimum clock period given by

$$t_{clk} + t_{skew} \geq t_{c\text{-}q} + t_{logic} + t_{su} \quad \text{.....2.13}$$

$$t_{hold} + t_{skew} < t_{c\text{-}q,cd} + t_{logic,cd} \quad \text{.....2.14}$$

$$t_{clk} - 2t_{jitter} \geq t_{c\text{-}q} + t_{logic} + t_{su} \quad \text{.....2.15}$$

$$t_{hold} + 2t_{jitter} < t_{c\text{-}q,cd} + t_{logic,cd} \quad \text{.....2.16}$$

The combined impact of skew and jitter results in following constraint,

$$t_{clk} + t_{skew} \geq 2t_{jitter} + t_{c\text{-}q} + t_{logic} + t_{su} \quad \text{.....2.17}$$

The equations from 2.13 to 2.17 illustrates that both skew and jitter affect the performance of system. The jitter has direct impact on maximum operating frequency of system because in worst case it decreases the usable cycle time and may result in critical path failure [37]. If the skew is increased beyond certain limit, it can violate the hold constraint, thus bringing about the races and thereby the malfunctioning of circuit [4]. Few researchers have proposed the H tree structure as a CDN. The H tree CDN assures minimum skew with balanced load, but with PVT variation, H tree also

exhibits a skew. Also, along with skew and jitter, clock slew have significant impact on timing parameters of flip flop such as set up time and hold time. The uncontrollable clock slew may cause up to 90% deterministic fluctuation in timing parameters such as setup time and hold time [38] thereby collapsing the functionality of system. Generally to assure the proper functioning of the system, in presence of the uncertainties, clock cycle is often stretched. But this in turn adversely affects the performance.

2.5.2 Performance Metrics of Clock Generator

Voltage Controlled Oscillator (VCO) is generally opted as a clock generator circuit [39]. The governing equation of VCO is given by 2.18.

$$F_{VCO} = f_o + K_{VCO} V_{ctrl} \qquad \text{…….2.18}$$

where, f_o is the free running frequency (centre frequency) of VCO, K_{VCO} is the gain of VCO and V_{ctrl} is the input to the VCO.

The two most commonly used topologies of VCO are the LC oscillator and the ring oscillator. The output frequency of LC oscillator is given by equation 2.19.

$$f = \frac{1}{2\pi\sqrt{LC}} \qquad \text{…….2.19}$$

where, L is the inductance and C is the capacitance of tank circuit. Thus, for moderate speed applications which require frequency in few tens of MHz, the corresponding values of L and C are larger and hence have larger size which results in integration difficulties. Moreover, LC oscillators have a narrow frequency tuning range specifically in low-voltage applications [39]. Kamalinejad et al suggested that ring oscillator based VCO is an attractive alternative because of its simple architecture, low area, wide tuning range and ease of integration [40]. In ring oscillators, an odd number of inverters are connected in loop to generate a periodic signal whose frequency is determined by the delay of each inverting stage. With differential delay stages, the ring oscillator can have even number of stages with feedback swapped. Even though the differential type ring oscillator is more immune to common mode noise such as supply voltage variation, it consumes more power and is more complex [4]. CSVCO configured using CMOS based ring oscillator is a good choice as it offers certain advantages like low power consumption, improved tuning range and

better phase noise performance [41]. The performance metrics of VCO includes tuning range, maximum frequency, power consumption, jitter, and robustness to PVT variations.

2.5.3 Performance Metrics of CDN

CDN is a network of wires which distributes clock signal to the clocked elements throughout the chip. Grid, H-tree, Spines are some of the CDN topologies. Grid exhibits lower skew between nearby clocked elements but, at the cost of increased metal resources and thereby increased power consumption. For balanced load, H-tree provides lower skew, lower routing resources, lower area and lower power consumption compared to the grid (Non tree) topologies [13]. However, H tree topology of CDN exhibits the sensitivity to process and environmental variations. Spines may exhibit large skew between the nearby elements which are connected to different serpentines.

CDN must be designed vigilantly to take care of the design parameters such as slew, skew, latency, susceptibility to PVT variation and power consumption. A CDN fed with clock generator via the large driver with no repeater (buffer) within distribution network is equivalent to a RLC line driven by CMOS driver. The propagation delay of a CMOS gate driving an RLC interconnect is a function of driver resistance, load capacitance, interconnect resistance, capacitance and inductance [42].

By virtue of technology scaling, the device dimensions are shrinking, die size and circuit speed are increasing, but the delay posed by the wire is becoming a dominating factor and therefore needs a considerable attention. In fact, in deep nanometer regime, the parasitic components of wire exhibit the scaling behaviour differently than that of device. It results in slower wires and faster device. Moreover, in strong inversion region, with technology scaling, the resistance of copper wires increases resulting in longer delays and electro-migration. Thus, in conventional strong inversion region the driver resistance is smaller as compared to the interconnect resistance. But, as voltage is scaled down to weak inversion region, a contradictory picture is observed. As V_{DD} is scaled below threshold voltage, the resistance of driver becomes very high compared to interconnect. Therefore, the driver resistance and interconnect capacitance are dominant in weak inversion region. Thus, in weak inversion region, the driver can be modelled as a resistor and interconnect as distributed capacitance as

shown in Figure 2.5. Since, the capacitance is a dominant parasitic component of interconnect in sub threshold region, to provide simplicity in analysis, the distributed capacitance of interconnect can be considered as lumped capacitance as shown in Figure 2.5 [4].

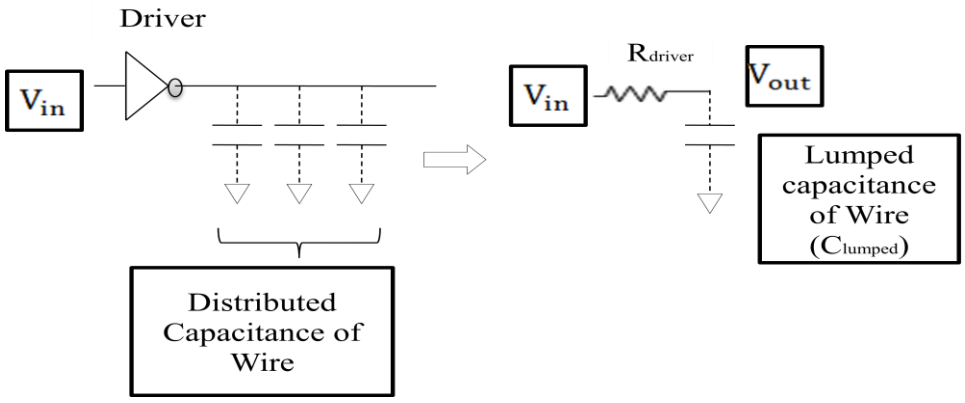


Figure 2.5: Model of Interconnect driven by driver in weak inversion region.

The equation of RC network in Figure 2.5 is given by 2.20.

$$C_{lumped}\frac{dV_{out}}{dt}+\frac{V_{out}-V_{in}}{R_{driver}}=0 \qquad \text{.....2.20}$$

where, C_{lumped} is the lumped capacitance of interconnect and R_{driver} is the driver resistance.

The transient response of the RC circuit for step input V rising from 0 to V volts is given by,

$$V_{out}(t)=(1-e^{\frac{-t}{\tau}})V$$

where,

$$\tau = R_{driver}C_{lumped}$$

The time to reach 10% of maximum input voltage for RC network is,

$$t_{10\%}=\ln(1.1)\tau$$

The time to reach 90% of maximum input voltage for RC network is,

$$t_{90\%}=\ln(10)\tau$$

The clock slew is,

$$Slew=\ln(10)\tau-\ln(1.1)\tau$$

$$Slew=2.2\tau \qquad \text{.....2.21}$$

Thus, slew degradation of clock signal from initial point to final point in sub threshold regime is a function of time constant τ, which is a product of driver resistance and interconnect capacitance. Conventionally, in order to satisfy the slew constraint, many small repeaters (buffers) are placed within the distribution network.

Such a CDN is referred to as buffered CDN. For buffered tree, output slew of buffer is given by equation 2.22 [43].

$$Slew_{out}(B) = K_{cap}^{slew} Cap_{out} + K_{slew} \quad \text{.....2.22}$$

where, K_{cap}^{slew} is the coefficient of output capacitance for slew computation and K_{slew} is the intrinsic output slew. Thus, equation 2.22 shows that the output slew is a strong function of output capacitance. It depends on drive current and output capacitance.

Delay of the clock buffer in buffered tree in terms of slew is given by equation 2.23 [43].

$$D(B) = K_{slew}^{delay} Slew_{in}(B) + K_{cap}^{delay} Cap_{out}(B) + K_{delay} \quad \text{.....2.23}$$

where, K_{slew}^{delay} is the coefficient of input slew, K_{cap}^{delay} is coefficient of output capacitance, K_{delay} is the intrinsic delay of the buffer.

The spatial variation in arrival time of clock transition at different clocked elements is referred to as clock skew. The delay taken by clock signal to move through CDN to the clocked elements is called as latency. Variation in latency can be termed as skew.

For H-tree buffered network, latency is given by equation 2.24.

$$T_{delay} = T_{H\text{-}tree} + T_{Driver} \quad \text{.....2.24}$$

$T_{H\text{-}tree}$ is given by equation 2.25 and delay of buffer (T_{Driver}) in sub threshold regime with output capacitance C_L is given by equation 2.8. Thus the sources of variation in buffered H tree are the variation in interconnect parameters viz. length, width and spacing of the wire as well as variations in driver (buffer).

For H-tree un-buffered network, latency is given by 2.25 [44].

$$T_{H-tree} = 0.4\left(\frac{\rho.\varepsilon_r}{H_{int} T_{ILD}}\right) D^2 \left(1 - \frac{1}{2^{n/2}}\right)^2 + \frac{\sqrt{\varepsilon_r}}{c_o} D\left(1 - \frac{1}{2^{n/2}}\right) \quad \text{.....2.25}$$

Where, ε_r is relative dielectric constant, c_o is speed of light in free space, H_{int} is the interconnect thickness, T_{ILD} is inter level dielectric thickness, n is H tree level, ρ is line resistivity and D is die size.

For un-buffered network, the source of delay between clock generator and clocked element is only wire. Thus, for un-buffered H tree the only source of variation, as

indicated by equation 2.25, is the variation in interconnect parameters viz. length, width and spacing of the wires.

2.5.4 Review of Low Power Clock Circuit

Various oscillator topologies with different tuning techniques for clock generators have been proposed in the past by the researchers [41, 45]. Off-chip components such as crystal oscillators can provide a very stable clock, but are not suitable for energy constrained systems mainly because of their large size and higher power consumption. LC oscillators are also popular because of their superior phase noise properties. However because of difficulty of integration of passive components, LC oscillators found limited use in applications where area is an important constraint. By using a RC relaxation oscillator described in [45], the power consumption can be reduced. However, a large area is required by the on-chip resistors and capacitors. These passive components consume large area and are not accurate, resulting in the increase of chip cost and inaccuracy of frequency thereby decreasing reliability. Current starved ring oscillator configured using CMOS based ring oscillator is a good alternative as it offers certain advantages like low power consumption, improved tuning range and better phase noise performance [41].

The challenge in designing on chip CMOS clock generator is to achieve low power, minimal area and frequency stability in presence of PVT variations. Various methodologies have been proposed by the researchers to address these issues in super threshold regime [46-53]. Although substantial work to mitigate the design issues of clock generator have been proposed in conventional super threshold regime, a very few researchers have explored this area in sub-threshold regime. W. Rim, W. Choi, J. Park proposed an adaptive clock generator circuit [54]. Researchers have reported a promising approach of solving the timing problems using the clockless asynchronous design [55]. However, due to lack of Computer-Aided Design (CAD) tools for the synthesis and optimization of asynchronous circuits, the implementation of the asynchronous systems faces many design difficulties [56]. Researchers have proposed a two stage ring oscillator designed at 90nm CMOS technology [57]. The proposed oscillator had its delay cell biased in weak inversion region and generated oscillation signals at 5.12 MHz with 0.3 V power supply. Researchers have proposed a sub threshold ring oscillator based temperature sensor [58]. This temperature sensor

exploited the temperature dependence of threshold voltage and mobility of MOS transistor. ULP oscillator with temperature and process compensation was reported by the researchers [59]. The proposed circuitry produced frequency of 1.28 MHz and variation of ±3% in its output frequency over a temperature range of -40˚C to 85˚C and consumed 1.18μW power.

Overall, very few reported ULP oscillators have addressed the sensitivity issue of clock circuit with respect to the environmental variations. Although, significant work has been carried out by the research community to combat the impact of temperature variation in the super threshold region [60-61, 46-47], very few researchers have explored this area in the sub-threshold regime. Moreover, very few researchers have focussed on low power temperature insensitive circuits [62-65]. To have temperature insensitive circuits, researchers have proposed the use of the bootstrapping technique [62]. The use of external components to implement temperature insensitive circuits has been proposed by the researchers in [63-64]. The comparators and S-R flip flops are used to have temperature insensitive circuits by the researchers in [65]. However, the power consumption is still several microwatts and the frequency is in KHz. Researchers have proposed a low power temperature monitoring circuit with some transistors in sub threshold and some in super threshold region [23]. Therefore to implement the circuit, two power supplies were required, which made the circuitry complicated and increased the power consumption.

Thus, the exponential dependency of clock period on temperature and increasing demand to have ULP circuits compels one to devise the simple techniques to design the sub threshold ring oscillator with reduced thermal sensitivity. Moreover, the exponential sensitivity of transistor operating in sub-threshold domain, makes it highly prone to process, and temperature variations and hence poses problems to the clock circuit design. PVT variations brings about deviation in delay which is reflected in variation of rising and falling pulse edges referred to as jitter thereby threatening the frequency stability of clock generators.

Technology scaling is becoming increasingly challenging in deep nano-meter regime. International Technology Roadmap for Semiconductors (ITRS) has predicted that in nano-meter regime, the expected high integration will encounter substantial difficulties, possibly preventing the continued improvements in figures of merit, such as low power and high performance. Novel transistor structures and new material

such as strained Silicon and new channel material to provide high mobility are extensively explored by the researchers to see both performance and power benefits. FinFET and CNFET technology exhibits improved performance and are the promising alternative to the CMOS technology. The degraded performance of sub threshold circuits obstructs its wide applicability. In order to have energy efficient circuits with better performance, it is vital to explore the performance of emerging devices like CNFET and FinFET in sub threshold circuits. Researchers have focused on design of FinFET VCO in super threshold regime. Parameters of novel VCO built using independent gate DG-MOSFET is explored by the researchers [66]. Also recently researchers have investigated the viability of FinFET technology using a nano-scale current starved voltage controlled oscillator [67]. FinFET based VCOs are more robust and efficient compared to CMOS CSVCO in super threshold region [68]. Furthermore, FinFET VCO gives very high tuning range as compared to MOSFET [69]. However, it is not very clear that which configuration of DG FinFET will be efficient for CSVCO in sub threshold regime. The combination of different configuration of DG-FinFET, to seek the advantage of improved drive current of SG mode and reduced capacitance of IG mode, may give fruitful results for the critical circuits like VCO in the sub threshold region.

CNFET has been investigated by the researchers for analog as well as digital circuits [70-71]. Researchers have investigated the performance of CNFET based inverter and proclaimed that he CNFET inverter exhibits good I-V characteristics [70]. The research work has demonstrated multistage complementary NOR, OR, NAND, and AND logic gates and ring oscillators at frequency 220 Hz with arrays of p- and n-type nanotube field effect transistors (FETs) [71]. Researchers have investigated the radio frequency (RF) and linearity performance of transistors using CNT and reported that CNFETs with semiconducting nano tubes are potentially promising building blocks for highly linear RF electronics and circuit applications [72]. CNFET technology has been combined with CMOS technology to provide hybrid structure which exhibits better performance [73-75]. Researchers have compared the performance of CMOS, CNFET and hybrid configurations and reported that, the hybrid PCNFET-NMOS configuration exhibit better performance [73]. The researchers have demonstrated a two transistor cascode amplifier using hybrid configuration with Silicon NMOS and CNT transistors [74]. A novel ultra low power

energy efficient hybrid Power-Gating (PG) method has been proposed by the researchers [75]. To improve the speed of CNFETs, various optimization schemes have been demonstrated by the researchers [76-77]. The dynamic response of CNFET based NOT gate was explored by researchers and their analysis indicated that the parasitic capacitances causes the degradation of CNFET based ICs [76]. The researchers have also recommended various optimization schemes to minimize the effect of parasitic capacitance and thereby improve the speed. The effect of different CNFET parameters on various performance characteristics was investigated by the researchers and they reported that performance improvement can be achieved by optimization of various CNFET parameters [77]. Researchers have proposed back gate biasing scheme to further enhance the characteristics of CNFET [75, 78-79]. Researchers have demonstrated CNFET based sub threshold SRAM cell and reported that back gate biasing improves the performance of sub threshold SRAM cell [78]. The researchers have compared the performance of Si MOSFET based and CNFET based SRAM cell [79]. The results have indicated that CNFET based SRAM cell exhibits better results compared to its MOSFET SRAM counterpart. CNFET and FinFET exhibit extraordinary properties like near ideal sub threshold slope, small gate capacitance and higher I_{on}/I_{off} ratio. Therefore, it is vital to investigate the viability of FinFET and CNFET for sub threshold clock circuit.

CDN in clock circuit can significantly affect the overall system performance and reliability [80]. Thus, while designing the clock distribution system utmost care must be taken to equalize the time between the clock generator and the clocked receivers. Global clock distribution networks can be classified as grids, H-trees, spines, or hybrid. A specific topology can be opted for a specific application as per its requirement to reduce the skew [13]. Moreover, CDNs are wire dominated networks and therefore characteristics of wire viz. interconnect greatly affects the clock signal passing through it. This large distributed network consumes significant amount of power. Further, various factors such as the systematic or random process variations and IR-drop have a large impact on the performance of a CDN. Technology scaling makes the global interconnects more resistive leading to larger delays, increased skew and reduced performance. Variability is another major problem posed by technology scaling. The unpredictable behaviour of this wire dominated CDN due to PVT variations makes CDN design more critical. Consequently, as a result of PVT

variations, the clock signal can have both spatial (skew) and temporal (jitter) variations leading to performance degradation and circuit malfunction [4]. The CDN must maintain the integrity of the signal and minimize parameters like clock skew, clock slew, jitter, and latency. It should of course be appended with minimal use of system resources such as power and area. Unfortunately, as chips are getting larger, wires are getting slower and clock loads are increasing. In this scenario, the distribution delay tends to go up even as cycle times are going down. Good CDNs can achieve low systematic skews, which were dominant component in the past, but random drift and jitter are posing major challenge in design of CDN. H-tree with numerous clock buffers is a commonly used topology to have identical timing characteristics. Conventionally in super threshold regime, researchers have proposed numerous techniques to minimize clock skew, slew, power consumption such as driver sizing, repeater insertion, interconnect width optimization, dynamic drivers, adding cross links, non tree CDN [81-87].

Driving large capacitive load of the clock networks with buffers operating in sub threshold regime creates a significant problem. Therefore, an efficient method to reduce skew and slew is important for viable sub threshold designs. Researchers have proposed a technique to control slew by having constraint on the load of the clock buffers at each level [38]. The researchers recommended that tighter nodal capacitance is essential to control the slew in sub-threshold CDNs.

The researchers have investigated and suggested the techniques to improve the performance of interconnects and thereby CDN from delay and power perspective. But along with low power requirement, robustness is essential requirement of a clock circuit. The unwanted random skew variations are not only harmful to timing performance but also difficult to control. PVT variation in the buffers can lead to substantial differences in drive strength that are essentially amplified by large loads, leading to potentially large clock skew. The uncontrollable clock slew may cause up to 90% deterministic fluctuation in timing parameters such as setup time and hold time [38] thereby collapsing the functionality of system.

The increased variation of gate delay in sub-threshold operation prominently leads to set up time violations [14]. To ensure the reliable operation safety margin needs to be added to the clock period, as there is an uncertainty component in the delay of every logic gate due to the PVT variations. This safety margin ensures a reliable

operation and decreases the probability of functional failure of the synchronous system. However, this results in degradation of performance of system. Alternatively, V_{DD} can be adjusted instead of the clock period. In this case the performance is improved but at the price of more power consumption. Employing practices like upsizing gate or utilizing grids to mitigate the variability problem increases power consumption thereby deviating from our ultimate goal of low power consumption. Therefore, there is a need to find the solutions to maintain the balance between power consumption, robustness and performance of clock circuit in sub-threshold domain.

2.6 Research Gap and Challenges

In the ubiquitous era of ULP applications such as wireless sensor nodes, pace makers, RFID tags, wrist watches, power consumption is a primary concern in order to extend the battery life. Clock circuit is a vital component in these applications. Since sub threshold circuits have huge potential to satisfy the ULP demand, design of clock circuit in sub threshold regime will eventually reduce the overall power consumption of these power sensitive applications. But degraded performance and exacerbated variability are major concerns in sub threshold regime. Despite the focus received by thermally aware design, very little work has been done to reduce hazards caused by temperature gradients in the ICs under sub-threshold conditions. Moreover, due to exponential sensitivity to PVT variations, robust design is an important concern for sub-threshold circuits. Furthermore, as technology scales down, it becomes more susceptible to PVT variations which contribute to the spread of clock cycle from its designed value. Emerging nano devices like FinFET and CNFET have great potential to supersede MOSFET. Hence it is vital to investigate the viability of these devices to improve the energy efficiency of clock circuit. Since, die size is increasing to incorporate maximum functionality in System on Chip (SOC) era, CDN is extending to cover larger area which results in more power consumption, degradation of slew and skew and therefore, it is vital to design energy efficient clocking circuitry with minimal slew and skew. Thus, the challenge in designing on-chip integrated CMOS clock system is to have robust and low power design simultaneously. Moreover, a well-designed, ULP robust clock system is a prerequisite for reliable circuit operation. However, a very few researchers have focused on designing a robust sub-threshold clock system. Therefore, there is a need to explore the challenges in design of sub threshold clock circuit and to investigate the techniques to mitigate the issues.

Chapter 3

DESIGN OF ROBUST CLOCKING CIRCUIT FOR MODERATE SPEED VLSI CHIP APPLICATIONS

3.1 Introduction

The clock circuit is one of the essential constituents of most of the digital circuit applications and it consumes significant power. Therefore, the design of ULP clock circuit has a great potential to reduce the overall power consumption of a system. This chapter deals with the design of various schematics of ULP clock generator circuit with CMOS and devices beyond CMOS. A scheme to improve the thermal stability of the sub threshold VCO is presented in this chapter. Furthermore, a strategy to reduce slew is discussed and slew aware CDN is designed.

In synchronous system the clock circuit plays an important role to decide the performance, reliability and power consumption of synchronous system. The ever increasing demand of portable electronics has compelled researchers to devise the techniques to achieve low power consumption. Sub threshold circuits have proven their ability to satisfy the demand of ULP consumption of battery operated applications. Thus, the challenges in designing ultra low power clock, in presence of degraded performance and magnified variability in sub threshold regime, needs to be investigated and different techniques to mitigate these challenges need to be explored.

3.2 Design of CMOS Based ULP CSVCO with H-tree Distribution Network

The simulation set up for clock system consists of a five stage CSVCO whose output is fed to D flip flop via un-buffered and buffered H- tree as shown in Figure 3.1 and Figure 3.2 respectively. CSVCO is opted for its low power consumption, improved tuning range and simple architecture. The H tree is selected because of its zero skew for balanced load and lower power consumption compared to non tree CDN. Even numbers of buffers are used between the clock source and load. Large central drivers are used at the output of clock generator to drive the un-buffered tree in order to satisfy the slew constraint which specifies that slew should not exceed 10-15% of clock period [43].

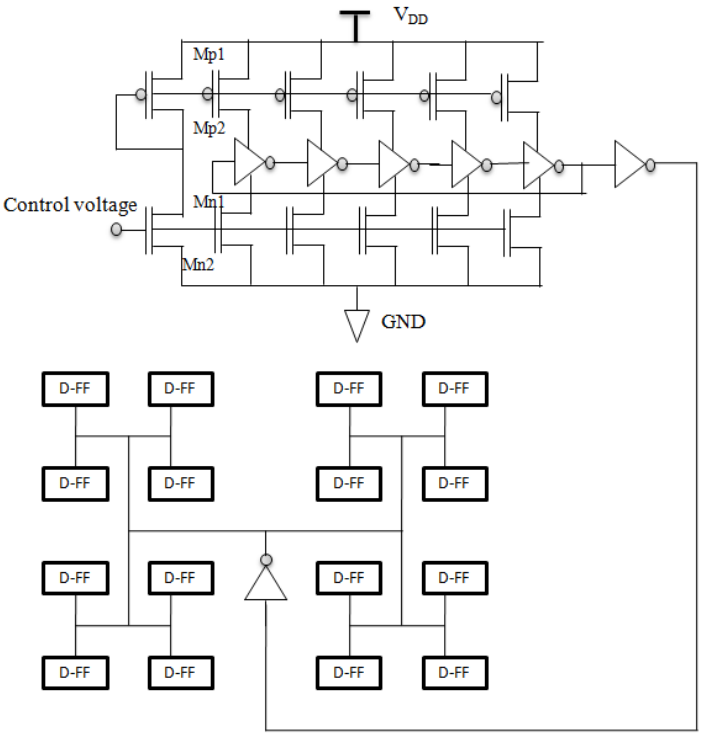


Figure 3.1: The clock circuit with un-buffered H tree

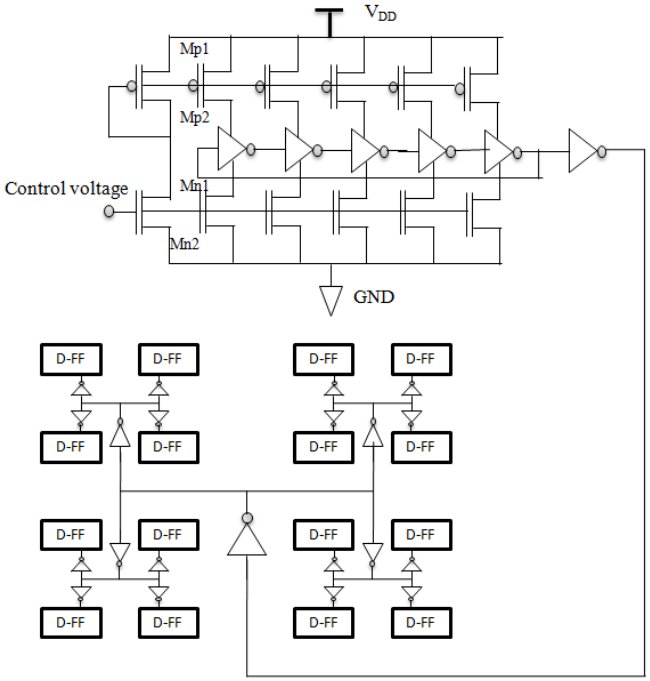


Figure 3.2: The clock circuit with buffered H tree

For clock system with buffered tree small buffers are distributed in H tree to satisfy the slew constraint. Both buffered and un-buffered clock systems are designed in such a way that they satisfy the slew and skew constraints and have comparable power consumption.

A two level H tree clock network with 16 D flip flops is designed for 1mm x1mm die size. At level 2, the interconnect length at chip horizontal axis (x) and vertical axis (y) is 166.66µm as given by equation 3.1 and 3.2 [88].

$$x = \frac{h}{2^{i+1} - 2} \qquad \text{.....3.1}$$

$$y = \frac{v}{2^{i+1} - 2} \qquad \text{.....3.2}$$

where, i is the number of H-Tree level, h is horizontal chip size and v is vertical chip size.

At level 1 the interconnect length at chip horizontal axis and vertical axis is $2x$=333.33µm and $2y$=333.33µm respectively [89]. These interconnect lengths are used for designing H tree. Conventionally, to have a uniformly tapered H tree, the conductor width in H-tree is progressively decreased in order to increase the resistance as signal propagates to higher level [80]. Figure 3.3 illustrates the dimensions for branches of H- tree used in simulation.

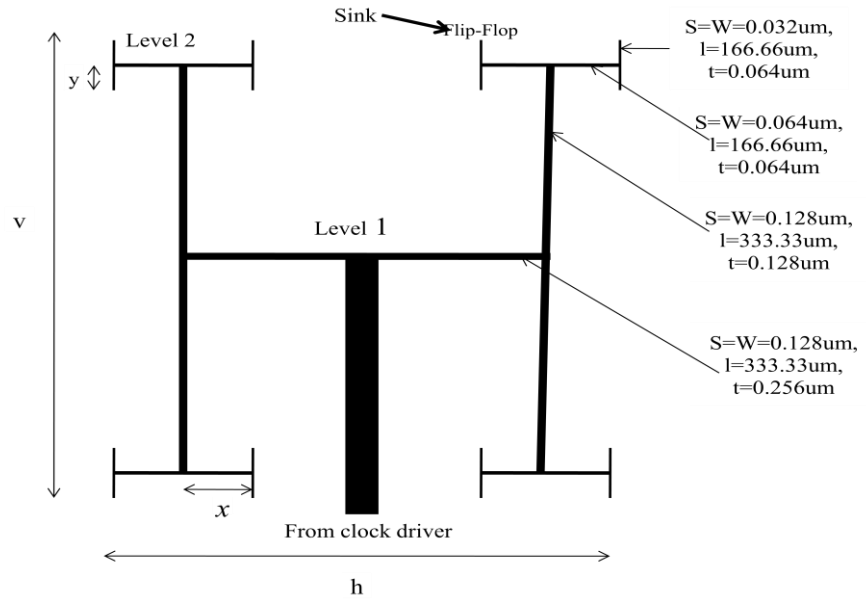


Figure 3.3: Tapered H Clock Distribution Network (design1)

The equivalent RLC model for Cu interconnect is shown in Figure 3.4.

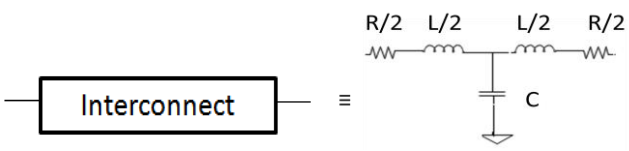


Figure 3.4: RLC model for Cu interconnect

The RLC parameters of Cu interconnect are extracted from Predictive Technology Model (PTM) [90] for Cu interconnects. The simulation is carried out using HSPICE at 32 nm technology node for both clock systems with un-buffered H tree as well as with buffered tree. Table 3.1 specifies some of the device parameters at 32nm technology node.

Table 3.1: 32 nm Berkeley Predictive Technology Model (PTM) device parameters

Parameter	**NMOS**	**PMOS**
Lg (nm)	32	32
Oxide Thickness (nm)	1.1	1.2
Threshold voltage (V)	0.49396	-0.49155

The set up shown in Figure 3.1 and 3.2 is used to explore the impact of lowering V_{DD} on various clock circuit parameters.

3.2.1 Design Methodology to Reduce Slew

This section attempts to improve the slew parameter of un-buffered CDN in sub threshold regime by redesigning the H-tree. Un-buffered CDN is a wire dominated network and therefore characteristics of wire greatly affect the clock signal passing through it. Interconnect design parameters, width (W) and spacing (S), were used by the researchers [91] for optimization of global interconnects in super threshold regime. Since, electro migration is a major concern for conventional super threshold interconnects, the thickness of super threshold interconnects is often kept larger to reduce the problems due to electro migration. On the contrary, electro migration is not a problem in sub threshold regime and therefore, thickness can be reduced while maintaining the aspect ratio. Researchers in [35] concluded that reducing width and/or thickness to width aspect ratio by one half can offer up to the multiple of 1.5-2 improvement in delay of sub threshold circuits. Thus instead of going by conventional method of progressively decreasing width at higher levels to increase the resistance in tapered H tree, thickness parameter can be employed to increase the resistance at higher levels. If thickness parameter at higher level of H tree is reduced, correspondingly its resistance will increase and capacitance will decrease. Moreover, slew is a strong function of capacitance and therefore the point where the clocked element is connected should have minimal capacitance [38]. Thus, reducing the

thickness at higher level of H tree to which clocked elements are connected will achieve decrease in capacitance. This reduction in capacitance of H tree at the nodes, where clocked elements are connected, will further improve the slew. Figure 3.5 illustrates the new dimensions of H tree with this strategy.

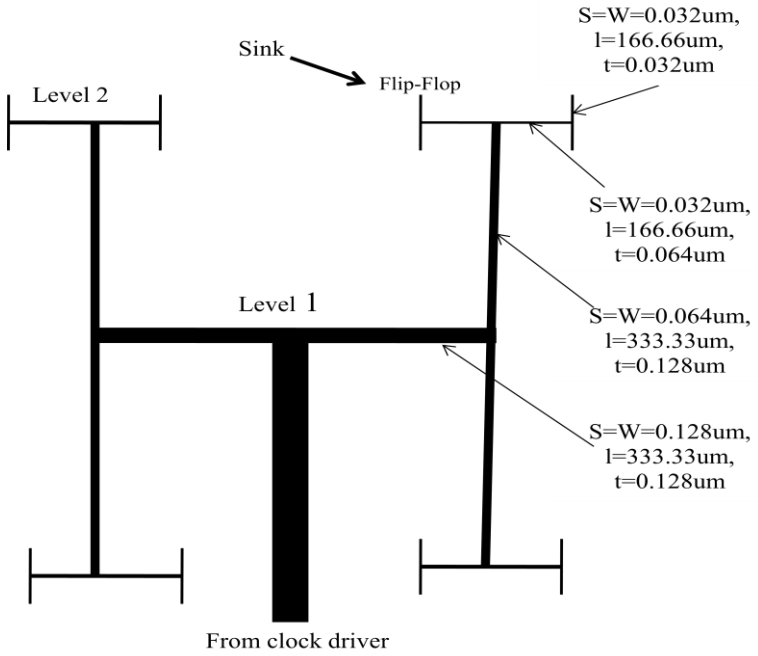


Figure 3.5: Tapered H Clock Distribution network (design2)

Accordingly with the above strategy, the H tree is redesigned and simulation is carried out to explore the parameters of clock system for this new design (design2) and is compared with clock system with H tree design discussed in previous section (design1).

3.2.2 Observations

The effect of scaling down of supply voltage on slew has been observed for buffered as well as un-buffered tree. It is found that the slew with buffered tree is better compared to un-buffered tree in strong as well as weak inversion region. The effect of supply voltage scaling on latency has been observed. It is found that the latency is a function of supply voltage for the buffered tree and it is independent of the supply voltage for the un-buffered tree in sub-threshold regime.

The consumption of the power for the CMOS circuit as a function of supply voltage is also measured. The un-buffered tree consumes slightly more power than buffered tree in strong inversion region.

An ideal clock circuit is expected to generate a periodic clock signal which synchronizes various clocked element. Unfortunately, clock signals are never ideal and are vulnerable to process variations. Along with the process variation, exponential dependency of sub threshold drive current on supply voltage and temperature makes the sub threshold circuits extremely sensitive to environmental variation. And hence the impact of process and PVT variation on the performance of buffered and un-buffered clock system is also observed. The performances parameters of CDN with variation of interconnect parameters such as width, thickness of wire and inter wire spacing at different supply voltages are also plotted. The effect of variations in device PVT parameters and interconnect parameters on slew and latency have been observed.

It has been seen that the clock system with un-buffered tree exhibit better latency, skew and robustness compared to the buffered tree in sub-threshold regime whereas buffered tree exhibits better slew. An attempt to improve the slew parameter for un-buffered tree is made by redesigning the tapered H tree CDN. The detailed results and discussions are presented in chapter 4.

The pulse width variation with device process and PVT variations is observed for clock system with buffered and un-buffered tree at varying supply voltage. The observation reveals that clock generator itself is dominating source for pulse width variation. Therefore techniques need to be devised to design stable VCO in sub threshold regime. Sub-Dynamic Threshold MOS (DTMOS) logic is one of the techniques to achieve stability against process and temperature variation and to enhance the switching frequency. The next section deals with the design of DTMOS based VCO circuit

3.3 Design of DTMOS Based Robust ULP CSVCO with Enhanced Performance

3.3.1 Conventional CMOS CSVCO

CSVCO is a ring oscillator based VCO in which the current sources limit the current available to the inverter. Figure 3.6 shows the schematic of CSVCO, in which I1-I5 are CMOS inverters, while MN12-MN16 and MP12-MP16 operate as current sinks and sources respectively.

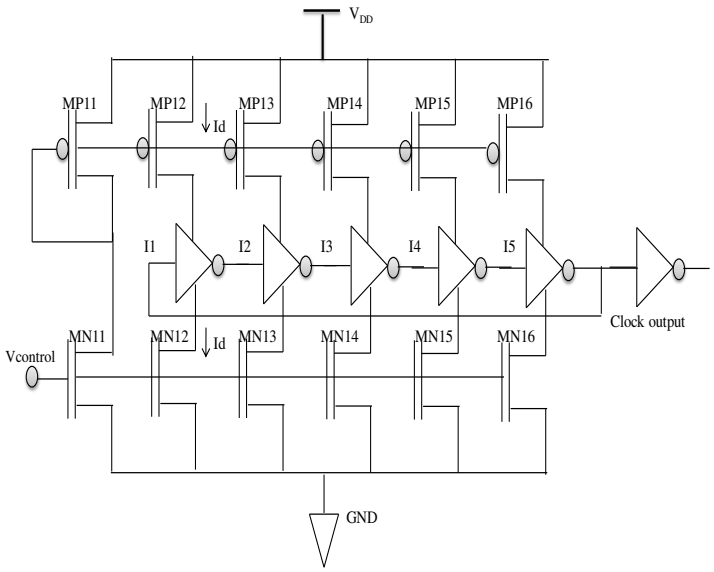


Figure 3.6: Schematic of CSVCO

The drain currents of MN_{11} and MP_{11} are set by the input control voltage. The currents in MN_{11} and MP_{11} are mirrored in each inverter/current source stage. Consequently the change in control voltage, $V_{control}$ induces a global change in the inverter currents and it affects the frequency of output of the VCO.

The total time period of the output pulse of CSVCO is given by equation 3.3 [10].

$$t_p = \frac{NC_{total}V_{DD}}{I_D} \qquad \text{…….3.3}$$

The CSVCO frequency is,

$$f_{osc} = \frac{I_D}{NC_{total}V_{DD}} \qquad \text{…….3.4}$$

where, I_D is the drive current, C_{total} is the load capacitance and V_{DD} is the voltage swing of the oscillator.

The V-I characteristics in the weak inversion region is modeled as 3.5.

$$I_D = I_0 e^{\frac{(V_{GS}-V_{th})}{nV_T}} \qquad \text{…….3.5}$$

where, V_{GS} is the gate to source voltage, V_{th} is the threshold voltage, I_0 is the current that flows when $V_{GS}=V_{th}$, V_T is the thermal voltage, 'n' is the sub threshold slope factor.

The threshold voltage of MOSFET is given by equation 3.6.

$$V_{th} = V_{tho} + \gamma\left(\sqrt{|\varphi_S - V_{bs}|} - \sqrt{\varphi_S}\right) \quad \text{.....3.6}$$

$$V_{tho} = V_{FB} + \phi_s + \gamma\sqrt{\phi_s} \quad \text{.....3.7}$$

where, V_{bs} is the bulk-source voltage, V_{tho} is the threshold voltage for $V_{bs} = 0$, γ is body effect factor, φ_s is surface potential and V_{FB} is the flat band voltage [8].

The time period and thereby the operating frequency of CSVCO depends on drive current as indicated by equation 3.3 and 3.4. The drive current in sub threshold regime however depends exponentially on threshold voltage and temperature as seen from equation 3.5. The exponential dependency of the sub threshold current on threshold voltage, which in turn depends on temperature and process parameters, makes the sub threshold circuits extremely sensitive to process and temperature variations. Sub-DTMOS logic is one of the techniques to achieve stability against process and temperature variation and to enhance the switching frequency [7]. The gate of MOS transistor is tied to its substrate in DTMOS logic. As indicated by equation 3.6, threshold voltage of MOSFET depends on the bulk to source voltage. In DTMOS, since gate is connected to bulk, variation in gate voltage causes V_{bs} to vary and hence changes the threshold voltage in ON state. In OFF state, DTMOS behaves like the regular MOS transistor.

3.3.2 Design of Various Configurations of DTMOS based CSVCO

The various configurations of DTMOS based CSVCO explored in this work are:

- CSVCO with all MOS transistors in ring oscillator replaced by DTMOS transistors, keeping current sources and sinks as MOS transistor, DTCSVCO-1.
- Only current source and sink transistors replaced by the DTMOS transistors keeping MOS transistors in ring oscillator, DTCSVCO-2.
- All transistors in CSVCO replaced by DTMOS transistors, DTCSVCO-3.
- Alternate stages of CSVCO ring oscillator with MOS and DTMOS transistor, DTCSVCO-4.

A five stage CMOS based conventional CSVCO and various configurations of DTMOS based CSVCO are designed using HSPICE at 32 nm technology node using PTM [90] and investigated to explore the better configuration.

3.3.3 Observations

The pulse width, slew and energy efficiency of conventional VCO and various configurations of DTMOS based CSVCO have been observed to explore their performance. It is found that DTCSVCO-3 is having highest switching speed and least slew whereas DTCSVCO-2 exhibits better energy efficiency. Along with performance, it is also necessary to analyze the stability of subthreshold circuits against process and temperature variation since subthreshold circuits parameters are highly vulnerable to these variations. The effect of temperature variation on pulse width of CMOS CSVCO and DTCSVCO variants at different process corners are plotted. The simulation results indicate that DTCSVCO-2 and DTCSVCO-3 exhibits better robustness compared to other configuration. The observation reveals that DTCSVCO-2 proves to be energy efficient and exhibits better robustness compared to conventional CSVCO.

The temperature error of DTCSVCO-2 is 3423ppm/°C which is better compared to conventional CSVCO that exhibits temperature error of 6348ppm/°C. However, still sensitivity of DTCSVO-2 to thermal variations is quite high and therefore the design of thermally aware clock generator circuit needs to be focused.

3.4 Design of Thermally Aware ULP Clock Generator

CSVCO configured using a CMOS based ring oscillator offers certain advantages like low power consumption, improved tuning range, simple architecture, low area and ease of integration. However, despite of these advantages, one of the major limitations of the ring oscillator is its sensitivity to the temperature variations leading to jitter [62].

The increasing demand for incorporating more and more features in the portable electronic applications has led to higher density, higher computational speed and lower cost. CMOS device dimensions are continuously shrinking to satisfy this need [92]. However with the enhanced features, the complexity and power increases significantly and therefore, power has emerged as a forefront design metric. Thus, with technology scaling, the power density in advanced CMOS VLSI design is increasing, which in turn generates heat and hence leads to thermal gradient across the chip. Moreover, in order to optimize speed and power in modern VLSI chips, heterogeneous design paradigm is adapted where the conventional high performance

and low power circuits are incorporated together, leading to large on chip thermal gradients. The aggressive interconnect scaling further leads to higher current densities and thereby increase in chip temperature. Also, different dynamic voltage scaling and clock-gating techniques have contributed to large temperature gradients. V_{th} varies with temperature variation as indicated by equation 3.9. Moreover, the drive current in the sub threshold regime exponentially depends on V_{th} and V_T. Therefore, the circuit parameters like delay and power consumption that depend on drive current exponentially vary with temperature. Thus, the thermal variations lead to unpredictable behaviour of the circuit and sometimes may even lead to circuit failure. Therefore, thermal management becomes an important concern and thermally aware design becomes the utmost of importance for reliable operation.

3.4.1 Thermal Analysis of VCO

From equation 3.3 and 3.5, the time period of CSVCO operated in sub threshold regime is given by equation 3.8.

$$t_p = \frac{N\ C_{Tot}\ V_{DD}}{I_0\ e^{\frac{(V_{GS}-V_{th})}{nV_T}}} \qquad \text{…….3.8}$$

The temperature dependence of the threshold voltage V_{th} and the mobility μ of the MOSFET is given by equation 3.9 [13].

$$V_{th} = V_{th0} - KT \qquad \text{…….3.9}$$

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-m} \qquad \text{…….3.10}$$

Substituting I_0 in equation 3.8

$$t_p = \frac{N\,C_{Tot}\,V_{DD}}{\mu C_{ox}\frac{W}{L}(n-1)V_T^2 \exp\left[\frac{V_{GS}-V_{th}}{nV_T}\right]}$$

Substituting equation 3.9 and 3.10 in above equation

$$t_p = \frac{N\ C_{Tot}\ V_{DD}}{\mu(T_0)\left(\frac{T}{T_0}\right)^{-m} C_{ox}\frac{W}{L}(n-1)\frac{K^2T^2}{q^2}\exp\left[\frac{V_{GS}-V_{th0}+KT}{nKT}\right]}$$

The rate of change of the time period of a VCO with respect to temperature is

$$\therefore \qquad \frac{dt_p}{dT} = -C_1 \left\{ \exp\left(\frac{C_2}{T} - C_3 \right) \left[(2-m) T^{(m-3)} + T^{(m-4)} C_2 \right] \right\} \qquad \text{.....3.11}$$

Where

$$C_1 = \frac{N C_{Tot} V_{DD} q^2}{\mu(T_0) C_{ox} (n-1) k^2 T_0^{\,m} \frac{W}{L}} \quad , \qquad C_2 = \frac{(V_{th0} - V_{GS}) q}{nk} \qquad \text{and} \qquad C_3 = \frac{q}{n}$$

Equation 3.11 illustrates the exponential dependency of the time period of a CSVCO output on temperature in the sub threshold regime. The negative sign indicates that the rate of change of the time period is inversely related to the change in temperature.

Since the drain current is governed by the control voltage in a CSVCO, equation 3.8 can be written as,

$$t_p = \frac{N C_{Tot} V_{DD}}{I_0 \, e^{\frac{(V_{control} - V_{th})}{nV_T}}} \qquad \text{.....3.12}$$

Simplifying equation 3.12,

$$t_p = a \, \exp\left[-\frac{V_{control}}{nV_T} + \frac{V_{th}}{nV_T} \right] \qquad \text{.....3.13}$$

$$\text{where,} \quad a = \frac{N C_{Tot} V_{DD}}{I_0}$$

The rate of change of the time period of a VCO with respect to the VCO input voltage ($V_{control}$) is given by,

$$\frac{dt_p}{dV_{control}} = a \, \exp\left[-\frac{V_{control}}{nV_T} + \frac{V_{th}}{nV_T} \right] \left(\frac{1}{-nV_T} \right)$$

$$\frac{dt_p}{dV_{control}} = \left(\frac{a}{-nV_T} \right) \exp\left[\frac{V_{th} - V_{control}}{nV_T} \right] \qquad \text{.....3.14}$$

The negative sign in equation 3.14 indicates the inverse dependency of time period on the control voltage. Thus, as the control voltage ($V_{control}$) decreases, the total time period (t_p) increases and vice versa. Thus, the time period of the output pulse of a CSVCO can be controlled with its control voltage.

Therefore, if the temperature variation is monitored and accordingly the control voltage is altered, the temperature variation impact on the time period of a VCO can

be mitigated. The next section focuses on the proposed control circuit which consists of two parts; a temperature monitoring circuit and a control voltage generator circuit.

3.4.2 Control Circuit Design to Combat Temperature Variation Effect

Figure 3.7 shows the proposed control circuit to combat the effect of temperature variations. The novelty of this circuit is that all the transistors are operated in the sub threshold regime. Moreover, a simple circuit and low power are the two major requirements of the sub threshold circuit and the proposed circuit satisfies these requirements.

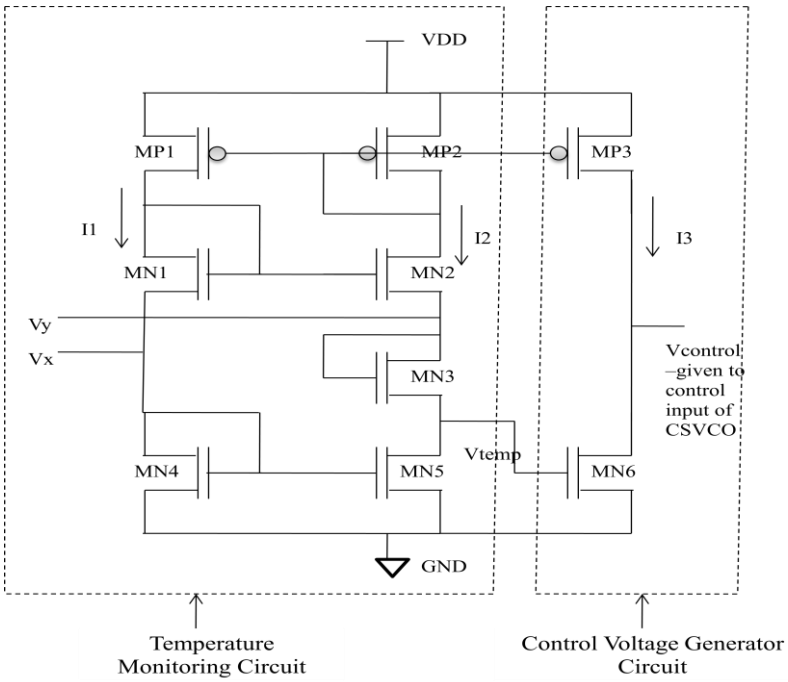


Figure 3.7: Proposed control circuit to combat temperature variation effect

MN_1, MN_2, MP_1 and MP_2 in Figure 3.7 constitute the current mirror circuit, which gives $I_1=I_2$. The control voltage which is to be given to the voltage controlled ring oscillator is obtained at the drain terminal of transistor MN_6. In order to ensure the equal source voltages of MN_1 and MN_2 and thereby $I_1=I_2$, V_x and V_y are kept at the same potential. All transistors, except the MN_5, are operated in the forward saturation region and transistor MN_5 is operated in the non saturation region in the sub threshold regime. The voltage at drain terminal of MN_3 is

$$V_y = V_{DS3} + V_{DS5} \qquad \text{…….3.15}$$

and

$$V_x = V_{DS4} \qquad \text{…….3.16}$$

$$V_x = V_y \qquad \text{…….3.17}$$

From equation 3.15, 3.16 and 3.17,

$$V_{DS4} = V_{DS3} + V_{DS5} \quad \text{…….3.18}$$

From Figure 3.7,

$$V_{DS4} = V_{GS4} \quad \text{and} \quad V_{DS3} = V_{GS3} \quad \text{…….3.19}$$

From equation 3.18 and 3.19,

$$V_{DS5} = V_{GS4} - V_{GS3} \quad \text{…….3.20}$$

The current I_1 and I_2 are given as,

$$I_1 = I_{01} e^{\frac{(V_{GS4} - V_{th})}{nV_T}}$$

$$\therefore V_{GS4} = nV_T \ln\left(\frac{I_1}{I_{01}}\right) + V_{th} \quad \text{…….3.21}$$

$$I_2 = I_{02} e^{\frac{(V_{GS3} - V_{th})}{nV_T}}$$

$$\therefore V_{GS3} = nV_T \ln\left(\frac{I_2}{I_{02}}\right) + V_{th} \quad \text{…….3.22}$$

From equation 3.20, 3.21 and 3.22,

$$\therefore V_{DS5} = V_{temp} = nV_T \ln\left(\frac{I_{02}}{I_{01}}\right) \quad \text{…….3.23}$$

And since $V_T = KT$, it is evident from equation 3.23 that V_{temp} is directly proportional to temperature and therefore it can be used as the temperature monitoring parameter.

MP_3 and MN_6 together constitute the control voltage generator circuit. The current of NMOS transistor, MN_6, is set by the control voltage V_{temp} generated by the temperature monitoring circuit. Therefore as the temperature increases, the V_{temp} increases which causes the drive current I_3 to increase, thereby decreasing the drain to source voltage of MN_6 i.e. the control voltage and vice versa. The overall proposed compensated CSVCO is shown in Figure 3.8. It is implemented at 32 nm technology node using PTM model parameters as given by Table 3.1.

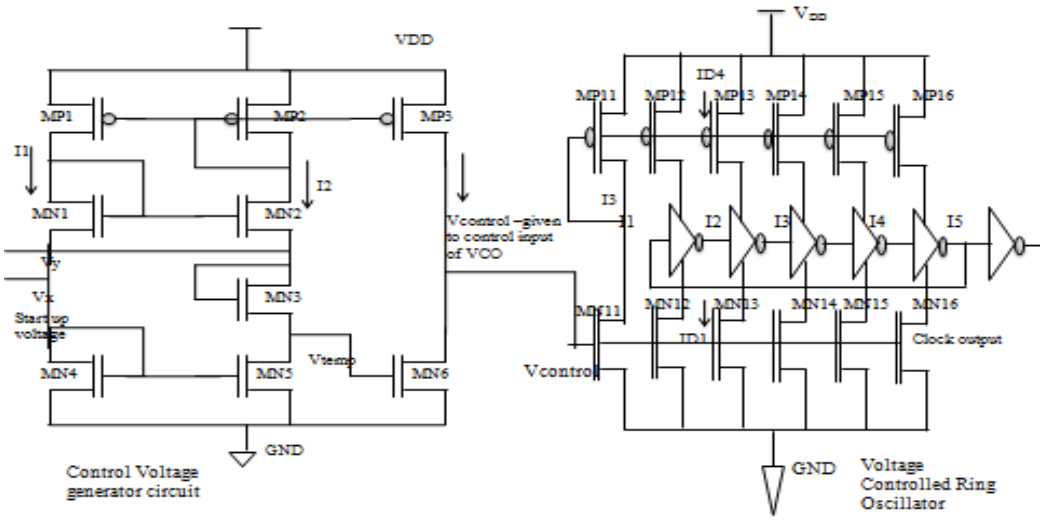


Figure 3.8: Proposed ULP voltage controlled ring oscillator with reduced temperature sensitivity

3.4.3 Observations

The pulse width variation of voltage controlled ring oscillator with temperature at super threshold 0.9V and sub threshold 0.3V are observed. It is found that the sub threshold ring oscillator is highly sensitive to temperature variation. The proposed compensated VCO is simulated at different supply voltages within the sub threshold regime. It is observed that by selecting optimal supply voltage, low temperature coefficients can be achieved. The observations indicate that the proposed system produces stable clock frequency over a wide range of temperatures as compared to the conventional CSVCO circuit with minimal increase in the power dissipation.

The observations in section 3.2 showed that the clock system with un-buffered H-tree exhibits better latency, skew and robustness compared to the buffered H-tree in sub-threshold regime whereas buffered tree exhibits better slew. The next section deals with the design of optimized, slew aware sub threshold CDN.

3.5 Design of Optimized Slew Aware CDN for ULP Applications

3.5.1 Optimization of Interconnect Parameters

Optimization of interconnect parameters can offer improvement in sub threshold circuit performance [35]. The interconnect parameters viz. width, spacing and aspect ratio are varied and its impact on slew is investigated by simulating the clock circuit

with uniform H- tree at 32nm technology node at 0.3V supply voltage and the results are shown in Figure 3.9, 3.10 and 3.11 respectively.

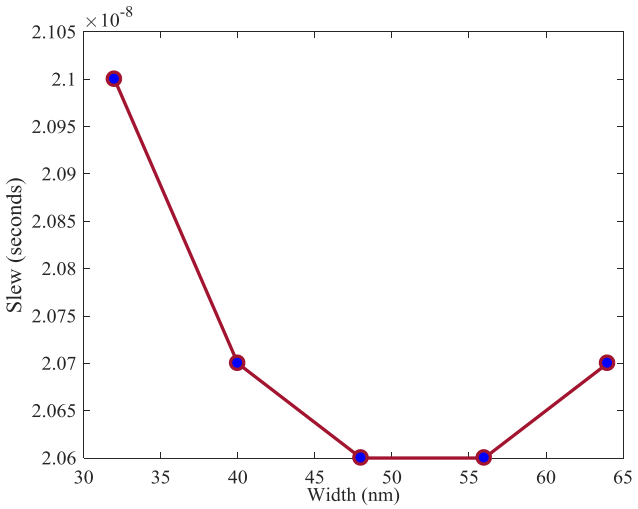


Figure 3.9: Impact of width variation on slew

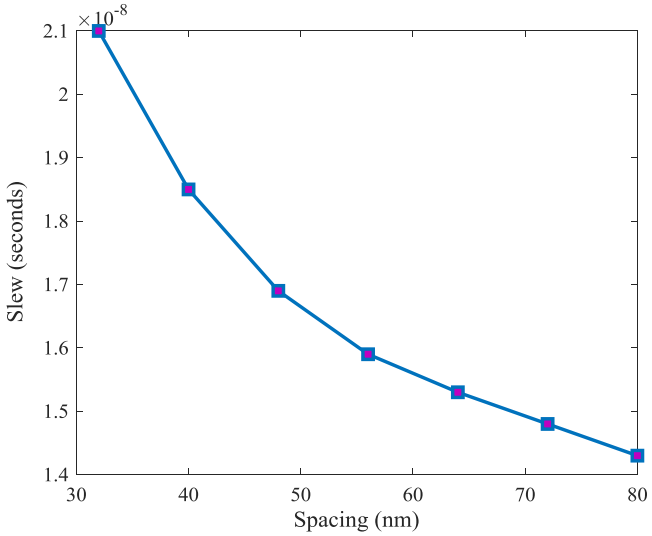


Figure 3.10: Impact of spacing variation on slew

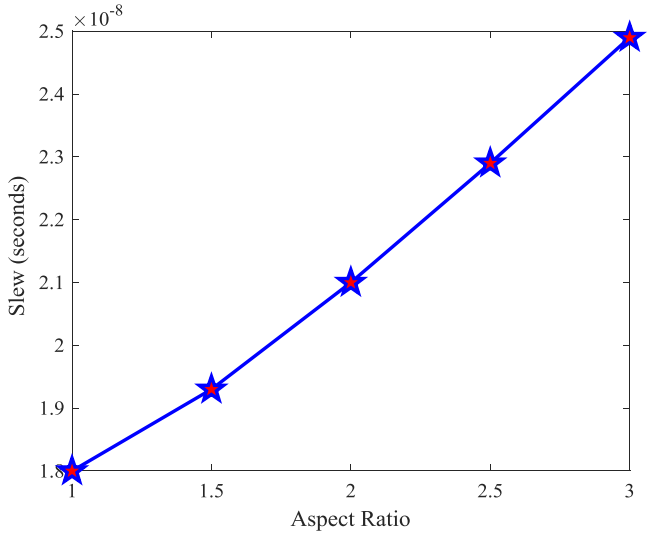


Figure 3.11: Impact of aspect ratio variation on slew

The RLC parameters for interconnect are derived from PTM. From these results the width, spacing and aspect ratio are selected to have the optimal value of slew.

3.5.2 Design Strategy to Improve Slew Parameter

The researchers have investigated the slew parameter and found that slew of clock is important only at the point of contact of CDN with clocked element, referred to as sink node, because slew is control signal for the clocked elements [38]. Thus, it can be concluded that, if a pair of inverting buffers is added only at sink nodes in H tree, it will improve the slew by increasing the drive current. The strategy adopted in this work is to improve the slew by inserting a pair of buffers only at the point of contact of CDN with clocked element with no buffers elsewhere in optimized uniform H-tree. The buffers added in the last stage are intended to increase the drive current for better slew. Also to ensure stable operation, variation in slew must be controlled.

As discussed in previous section sub-DTMOS logic demonstrates better stability in sub threshold regime. Therefore, in the proposed work the pair of buffers at the last level includes one DTMOS and one CMOS buffer added at the point where clocked elements are connected, with no buffers elsewhere in optimized uniform H- tree. Figure 3.12 depicts the various configurations in which buffers may be connected to the clocked elements.

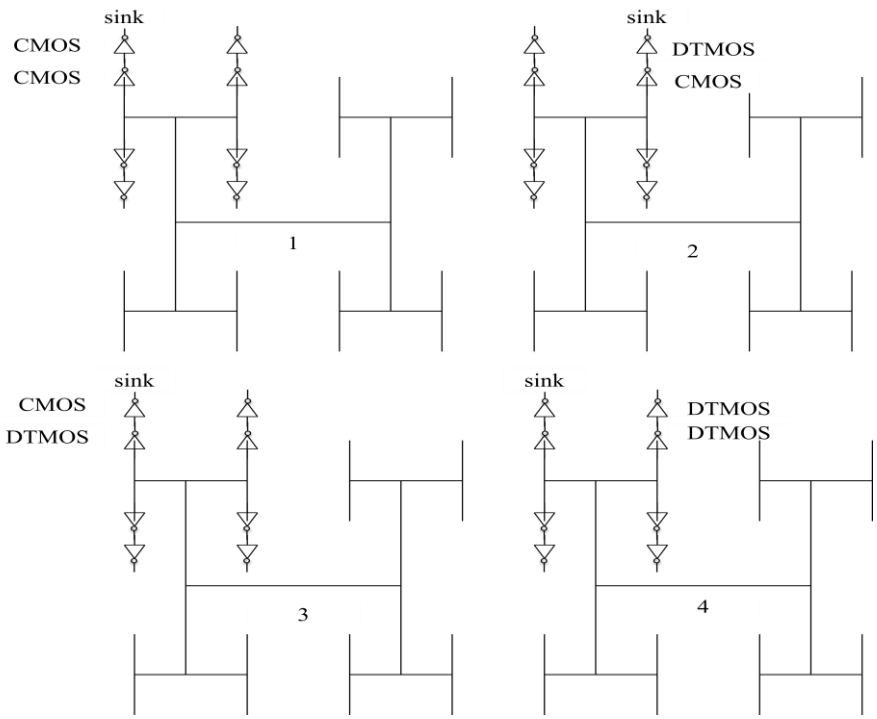


Figure 3.12: H tree with various configurations of buffers at sink nodes

Configuration 1 has both the buffers as conventional CMOS buffers, configuration 2 has DTMOS buffer connected to clocked element followed by CMOS buffer, configuration 3 has the conventional CMOS buffer connected to clocked elements, followed by DTMOS buffer, and configuration 4 has both DTMOS buffer in the last stage. These configurations are explored to investigate the configuration with better slew and robustness.

3.5.3 Observations

The slew parameter of the buffered and un-buffered tapered H-tree CDN for super threshold, near sub threshold and sub threshold region is observed. It is found that un-buffered tapered H-tree exhibits degraded slew for super threshold, near threshold and sub threshold region as compared to tapered buffered H-tree. Slew of optimized CDN with buffer at sink nodes in various configurations are observed. The observation indicates that optimized uniform CDN with configuration3 exhibits improved slew with additional benefit of reduced power consumption, compared to conventional CDN. Further, slew of conventional tapered un-buffered H-tree and optimized uniform H- tree with configuration3, for clock network designed for die size of 1mmx1mm, 2mmx2mm and 3.5mmx3.5mm, are observed. The variability of slew parameter with temperature variation at different process corners for conventional and optimized uniform H- tree with configuration3 is observed. The results are elaborated in Chapter 4.

The enormous obstacles posed by technology scaling such as increased sub threshold slope, random dopant fluctuations, mobility degradation, velocity saturation have decelerated the pace of technology scaling. Researchers have explored various structural modifications in the classical MOSFET structure and also have introduced new materials to confront with the challenges posed by technology scaling to sustain Moore's law. Fin-FET and CNFET are the promising alternatives which can supersede CMOS technology. The next sections deal with the exploration of FinFET and CNFET based clock circuits in sub threshold regime.

3.6 Design of ULP DG Fin-FET Based Clock Generator Circuits

Fin-FETs exhibits the near ideal sub threshold slope, small gate capacitance, higher I_{on}/I_{off} ratio [93]. Fin-FET circuits have lower functional power supply and lower optimal energy consumption compared to bulk CMOS [94-95]. Moreover, FinFETs

are promising alternative to bulk CMOS in nanometer regime due to its immunity to SCE's and reduced process variability.

3.6.1 Design of Various Configurations of DG Fin-FET based VCO

Double Gate (DG) FinFET can either be configured as a three terminal device which is also referred as Short Gate (SG) device, where the front gate and back gate are shorted or a four terminal device which is also referred as independent gate (IG) device. The SG and IG configurations of DG FinFET have their own pros and cons. SG double gate devices exhibits certain advantages like improved performance (almost double on current) and near ideal sub threshold slope [96-97] whereas IG double gate devices offer advantages like low gate capacitance, dynamic threshold voltage lowering, increased flexibility etc. [98-99]. The researchers have investigated that performance wise SG DG FinFET is better option while IG DG FinFET is an appropriate choice to ensure robustness [100]. Furthermore, reseaerchers in [100] proclaimed that SG DG FinFET can be an optimal choice in sub threshold regime, if robustness is ensured by application of some circuit level techniques. Thus at circuit level, various configurations may be employed to have a robust sub threshold circuit with better performance. The various configuration of DG FinFET considered in this study are–SG which implies tied gate option (3T) and IG implies untied gate (4T) in which back gate for N-DG FinFET is tied to ground and P DG FinFET is connected to supply voltage whereas front gate acts as a gate electrode. Also in this study, an IG configuration, with front gate as gate electrode and back gate of N DG FinFET connected to supply voltage whereas back gate of P DG FinFET connected to ground (MIGFET) is considered. Seven different CSVCO configurations are designed using above DG Fin-FET configurations and are enumerated below.

- CSVCO with all transistors in SG-DG FinFET configuration-SG CSVCO as shown in Figure 3.13.
- CSVCO with all transistors in IG-DG FinFET configuration-IG CSVCO as shown in Figure 3.14.
- CSVCO with transistors in ring oscillator in IG-DG FinFET configuration and current sources and sinks in SG-DG FinFET configuration-Hybrid CSVCO as shown in Figure 3.15.

- CSVCO with transistors in ring oscillator in SG-DG FinFET configuration and current sources and sinks in IG-DG FinFET configuration-Hybrid reverse CSVCO as depicted in Figure 3.16.
- All P transistors in CSVCO in IG configuration and N transistors in SG configuration-pignsg CSVCO as shown in Figure 3.17.
- All P transistors in CSVCO in SG configuration and N transistors in IG configuration-psgnig CSVCO as shown in Figure 3.18.
- CSVCO with transistors in ring oscillator in SG-DG FinFET configuration and current sources and sinks in MIGFET configuration-MIGFET CSVCO as shown in Figure 3.19.

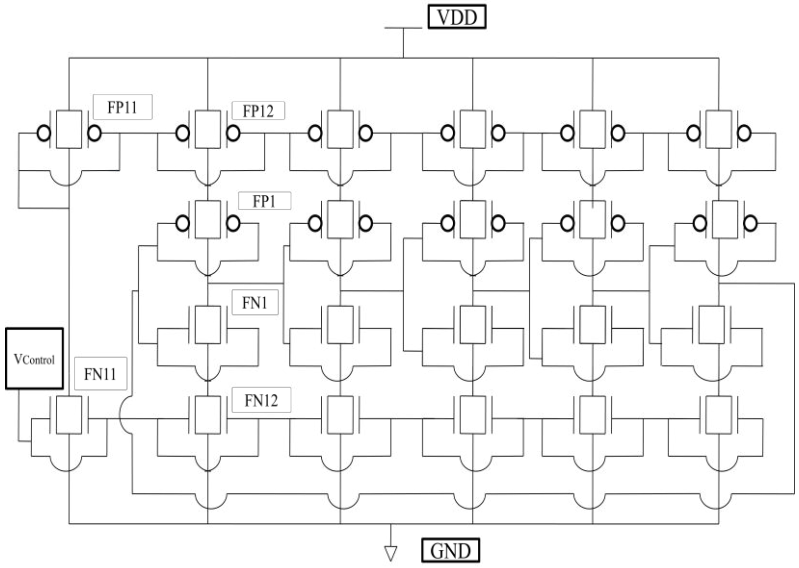


Figure 3.13: Schematic of SG CSVCO

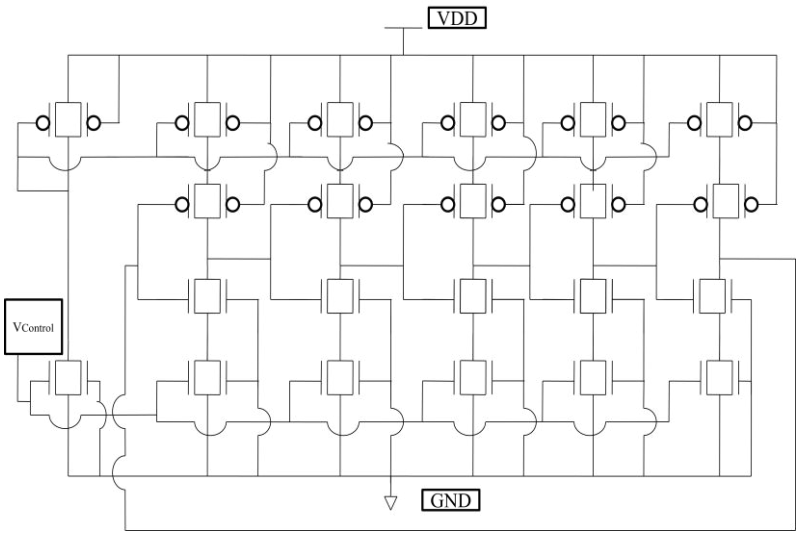


Figure 3.14: Schematic of IG CSVCO

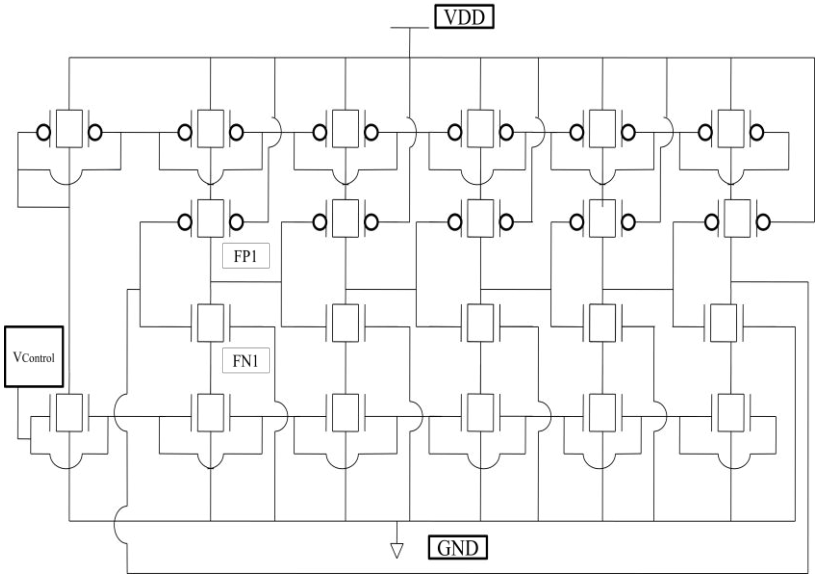


Figure 3.15: Schematic of Hybrid CSVCO

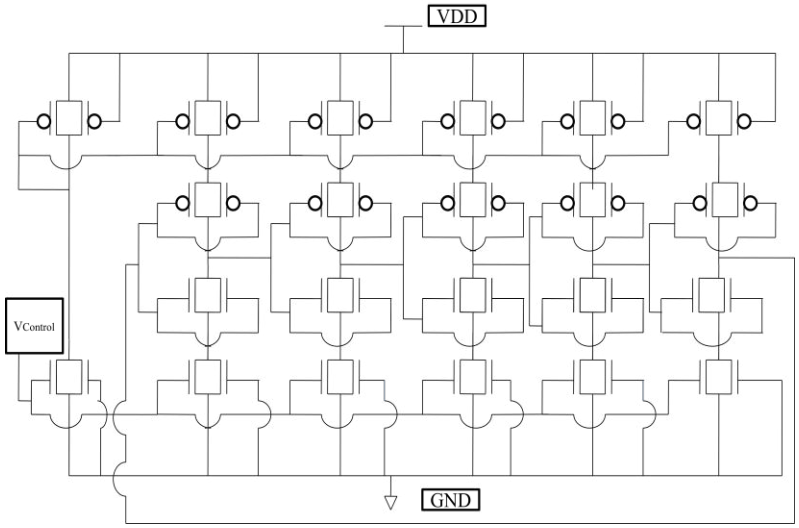


Figure 3.16: Schematic of Hybrid reverse CSVCO

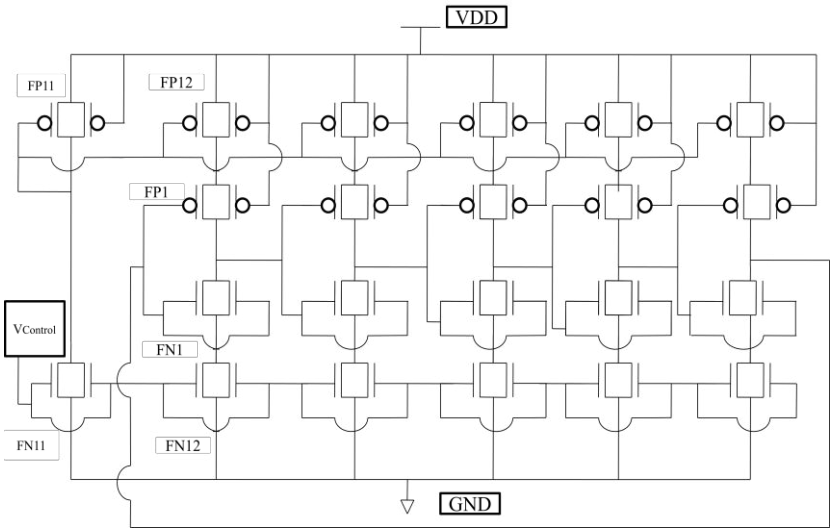


Figure 3.17: Schematic of pignsg CSVCO

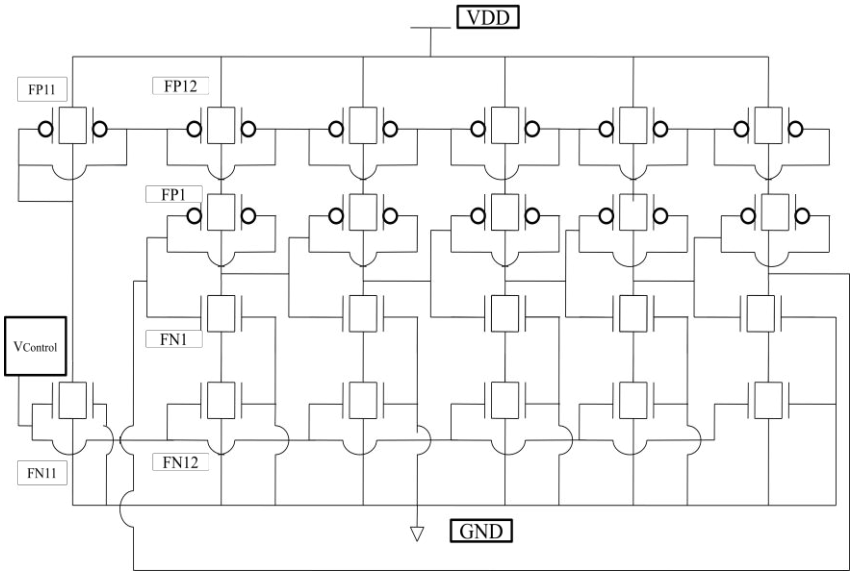


Figure 3.18: Schematic of psgnig CSVCO

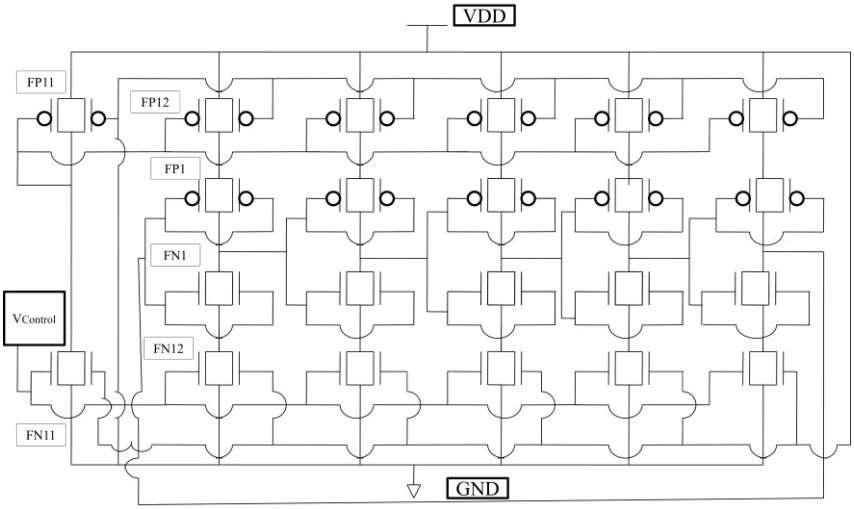


Figure 3.19: Schematic of MIGFET CSVCO

These seven configurations of DG Fin-FET based VCO are designed using HSPICE at 32 nm technology node using PTM model.

3.6.2 Observations

The performance of CMOS based CSVCO and SG DG-FinFET based CSVCO circuits in sub threshold region is observed. It is found that SG DG FinFET based CSVCO gives improved performance as well as robustness compared to bulk CMOS based CSVCO in sub threshold region. The performance of seven different configurations of FinFET based VCO are observed. It is observed that the enhanced charging current supplemented with reduced gate capacitance improves the PDP of pignsg and hybrid CSVCO. The variation in pulse width, PDP and EDP for the seven

configurations with variation in gate oxide thickness, body thickness, supply voltage and temperature are observed. MIGFET CSVCO exhibits better EDP; however, it is very sensitive to supply voltage variations. The results are discussed elaborately in chapter 4.

3.7 Design of CNFET Based Clock Generator in Sub threshold Regime

The extraordinary electronics properties of CNFETs such as excellent carrier mobility, near-ballistic transport, large current densities, scalability and improved sub threshold slope have steered the technology [101-109]. CNFETs are believed to be the most promising technology for future electronics in super threshold regime to extend Moore's law due to their outstanding performances [110-111]. CNFET are the FET with Carbon Nano Tube (CNT) as a channel. CNTs are sheets of graphene rolled in the forms of tubes. Depending on the chirality, the direction in which graphene sheets are rolled\, the single walled CNTs can be either metallic or semi conducting [112-113]. Also CNFETs are recommended as the promising alternative to CMOS technology by the International Technology Roadmap for Semiconductor (ITRS). Therefore it is vital to investigate the viability of CNFET for sub threshold clock circuit.

The chirality (C_h) of CNT is given by equation 3.24 and its relationship with diameter is given by equation 3.25 [114].

$$C_h = a\sqrt{m^2 + n^2 + mn} \qquad \text{.....3.24}$$

$$D_{CNT} = \frac{a\sqrt{m^2 + mn + n^2}}{\pi} \qquad \text{.....3.25}$$

Where, m and n are positive integers that specify the chirality of the tube, *a* (≈2.49e-10) is the inter-atomic distance between each carbon atom and its neighbor, D_{CNT} is CNT diameter

Threshold voltage of CNFET is given by equation 3.26,

$$V_{TH} = \frac{\sqrt{3}}{3}\frac{aV_{\pi}}{eD_{CNT}} \qquad \text{.....3.26}$$

Where V_{π} is the carbon π-π bond energy in the tight bonding model, e is the unit electron charge.

Equation 3.27 gives the relationship between band gap energy (E_g) and threshold voltage of intrinsic CNT channel.

$$V_{TH} = \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} \qquad \text{.....3.27}$$

The drain to source current in CNFET is given by equation 3.28

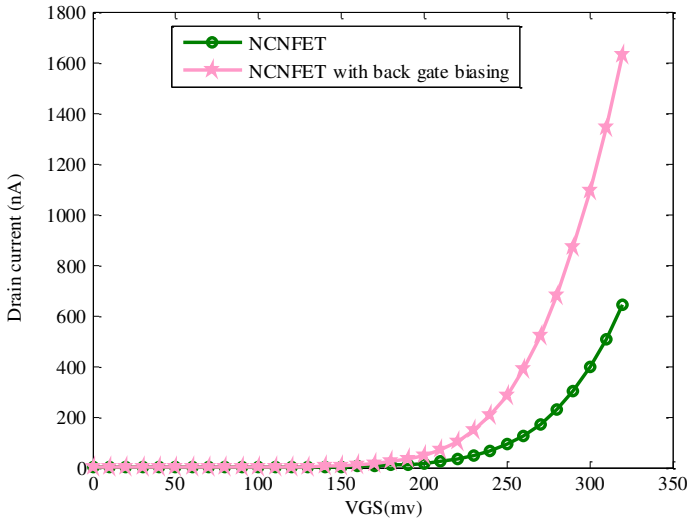
$$I_{CNFET} = \frac{Ng_{CNT}(V_{DD} - V_{TH})}{1 + g_{CNT}L_s\rho_s} \qquad \text{.....3.28}$$

Where g_{CNT} is the transconductance per CNT, L_s is the source length (doped CNT region), ρ_s is the source resistance per unit length of doped CNT, N is the number of nano tubes per device, V_{TH} is the threshold voltage.

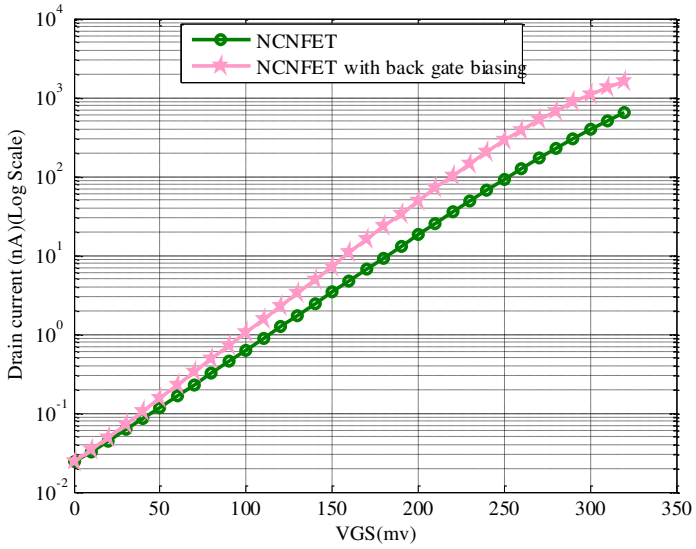
The conductivity of CNT depends on arrangement of carbon atoms which is decided by the chirality vector given by equation 3.24 and the chirality vector is related to diameter of CNT as indicated by equation 3.25. The threshold voltage is decided by diameter as shown by equation 3.26. Moreover source and drain series resistance is also affected by diameter. The drive current is affected by both threshold voltage as well as source resistance as indicated by equation 3.28. Therefore drive current is strong function of diameter.

3.7.1 Design of Various Configurations of CNFET based VCO

The sub threshold slope of CNFET with back gate biasing and without back gate biasing is investigated by simulating a 32nm NCNFET with varying gate to source voltage, for back gate=0V and back gate connected to gate. The value of chirality vector n,m is 17,0 respectively. Figure 3.20 (a) and 3.20 (b) illustrates the results.



(a)



(b)

Figure 3.20: Drain current variation for change in gate to source voltage

(a) Linear Scale (b) Log Scale

The results indicate that the sub threshold slope and performance of CNFET is improved with back gate biasing. Moreover the devices with better sub threshold are optimal for sub threshold circuits [115]. Therefore back gate biasing can be exploited to further enhance the performance of CNFET based CSVCO. Accordingly, using CNFETs with back gate biasing and without back gate biasing and its combination, four different configurations of CNFET CSVCO are designed.

These configurations are explored in this section and are listed below,

- CNFETVCO-1-In this CSVCO, the back gate of all NCNFETs is connected to ground and back gate of all PCNFETs is connected to supply voltage.
- CNFETVCO-2-The back gate of all CNFETs is connected to front gate in this CSVCO.
- CNFETVCO-3-In this CSVCO, back gate of all NCNFETs in ring oscillator is connected to ground and back gate of all PCNFETs in ring oscillator is connected to supply voltage whereas, back gate of all CNFETs in current sources and sinks is connected to front gate.
- CNFETVCO-4-In this CSVCO, back gate of all CNFETs in ring oscillator is connected to front gate whereas, back gate of all NCNFETs in current sinks is connected to ground and back gate of all PCNFETs in current sources is connected to supply voltage.

The schematic of CNFETVCO-1 of CNFETVCO-2, CNFETVCO-3 and CNFETVCO- 4 configuration are shown by Figure 3.21, 3.22, 3.23 and 3.24 respectively

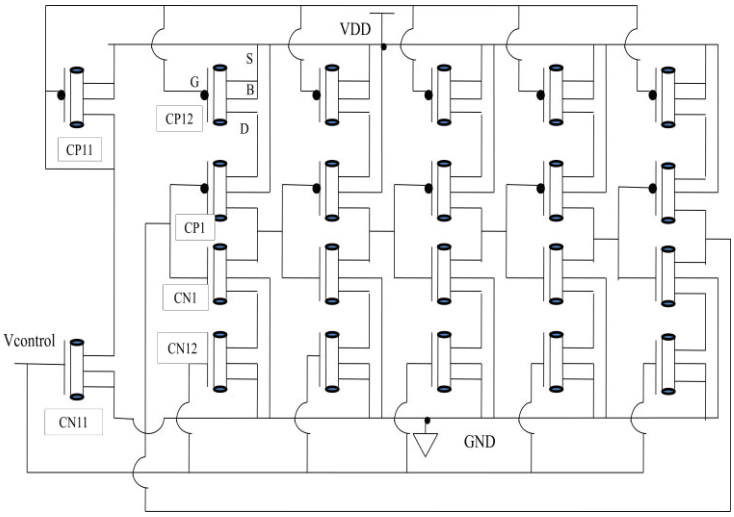


Figure 3.21: Schematic of CNFETVCO-1

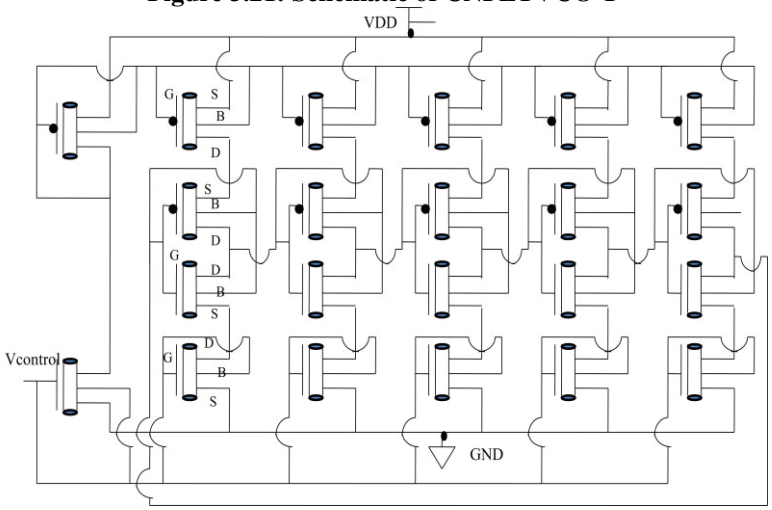


Figure 3.22: Schematic of CNFETVCO-2

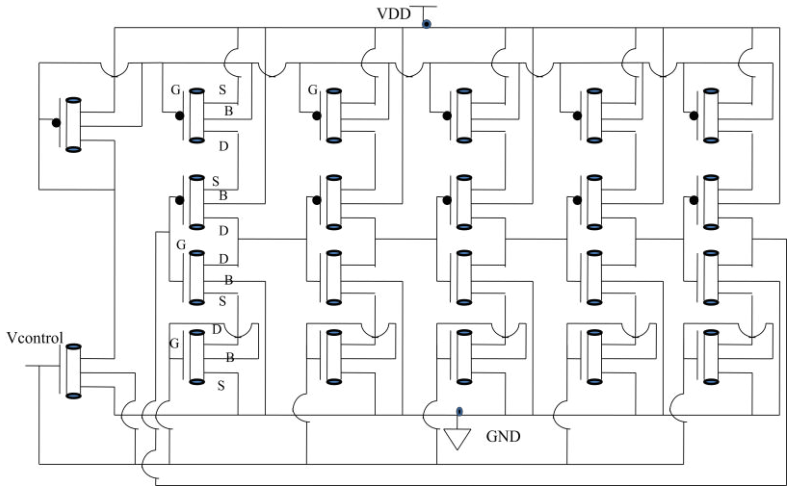


Figure 3.23: Schematic of CNFETVCO-3

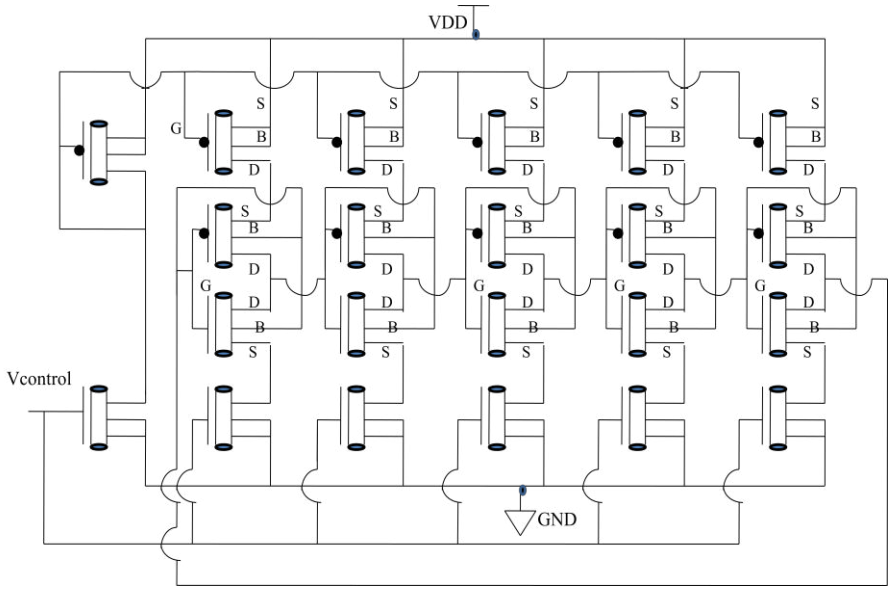


Figure 3.24: Schematic of CNFETVCO-4

These four configurations of CSVCO are designed at 32nm technology node with Stanford CNFET model [116] and are simulated in HSPICE. This CNFET model includes device parasitic components and the practical non-idealities such as the finite scattering mean path, the source/ drain series resistance, the source/ drain contact resistance, scattering etc. Table 3.1 and 3.2 illustrate the default parameter values used for CMOS and CNFET simulation respectively. A typical CNFET with planar HfO_2 gate oxide having thickness of 4 nm with a dielectric constant of 16 and SiO_2 substrate with dielectric constant of 3.9 is used for simulation in this work.

Table 3.2: Default parameter values used for CNFET simulations

Parameter	**Description**	**Values**
L_{ch}(nm)	Physical Channel length	32.0
K_{ox}	The dielectric Constant	16.0
T_{ox}(nm)	The thickness of dielectric material	4.0
Pitch(nm)	Distance between centre of two adjacent CNTs within same device	20.0
m,n	The chirality of tube	19,0
Tubes	Number of tubes in device	3

3.7.2 Observations

The performance and robustness of CNFET and CMOS based CSVCO are observed. It is found that CNFET VCO gives improved performance as well as robustness

compared to bulk CMOS based CSVCO in sub threshold region. The performance of different configurations of CNFET based VCO is observed. It is observed that the back gate biasing in CNFET improves the current but it also increases the gate capacitance. Therefore, CNFETVCO-3 with CNFETs in current source and sinks with back gate biasing and CNFETs in inverter without back gate biasing shows better output frequency and EDP compared to the other CNFETVCO configurations. The impact of supply voltage scaling on PDP and EDP of CNFET VCO variants is observed. Furthermore impact of temperature and chirality variation on pulse width of CNFET VCO variants is observed. The impact of variation in number of tubes, pitch, CNT diameter and oxide thickness on pulse width and PDP is plotted. The observed results are used to optimize various structural device parameters of CNFET and performance of optimized CNFETVCO-3 is evaluated. Monte Carlo simulations are performed to observe the overall impact of PVT variation on CNFETVCO output. Finally, the performance of CMOS VCO, DG FinFET pignsg VCO and optimized CNFETVCO-3 is observed. The results indicate that the CNFET based optimized CNFETVCO-3 exhibits better performance in terms of speed, energy efficiency as well as robustness. The results are discussed in detail in Chapter 4.

Chapter 4

RESULTS AND DISCUSSION

This chapter discusses the simulation results obtained by simulating various schematics of CMOS and devices beyond CMOS clock circuits that have been discussed in Chapter 3. It also investigates the suitability of conventional CDN for sub threshold regime and proposes a slew aware optimized CDN.

4.1 Performance Analysis of Impact of Supply Voltage Scaling on Clock System Parameters

The simulation set up consists of a five stage CSVCO whose output is fed to D flip flop via un-buffered H tree and buffered tree as shown in Figure 3.1 and 3.2 respectively in Chapter 3.

Figure 4.1 shows the impact of voltage scaling on slew for buffered and un-buffered tree. It shows that as the supply voltage of a clock circuit is scaled down from 0.9V to 0.2V, slew increases exponentially for buffered as well as un-buffered tree thereby hindering the performance in weak inversion region. This is because of the increased driver resistance and decreased drive current in weak inversion region.

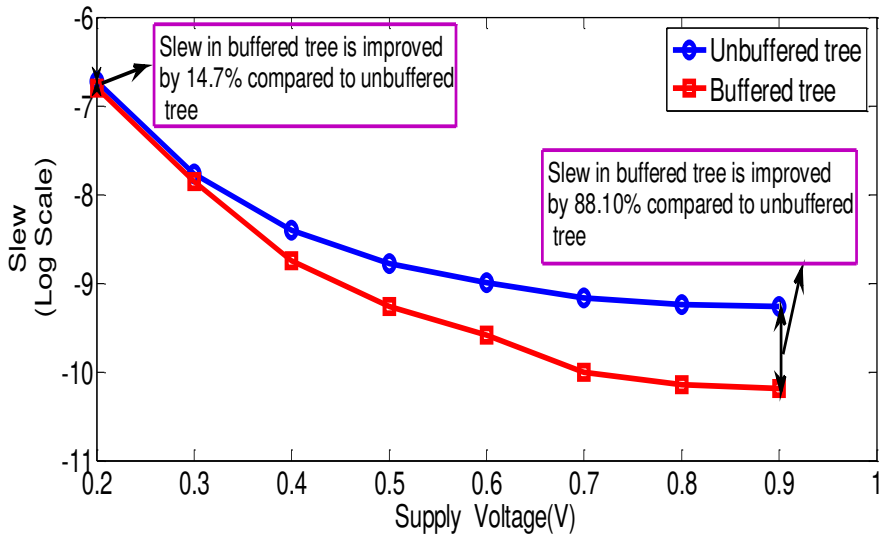


Figure 4.1: Impact of voltage scaling on slew

In conventional super threshold regime, the most popular strategy to improve the slew is to employ the buffers in CDN [117]. The advantage of using buffered tree in strong inversion region is evident from Figure 4.1, as slew for buffered tree improves

by 88% compared to the un-buffered tree. However, this advantage seems to be diminished as it goes towards the weak inversion region. Even though the slew with buffered tree is better compared to un-buffered tree in strong as well as weak region, the rate of increase in slew with supply voltage scaling for buffered tree is increased due to increased driver resistance.

Figure 4.2 shows the impact of voltage scaling on latency for buffered and un-buffered tree. Latency for clock system with un-buffered tree remains constant with supply voltage scaling whereas the latency for buffered tree increases exponentially in sub threshold region.

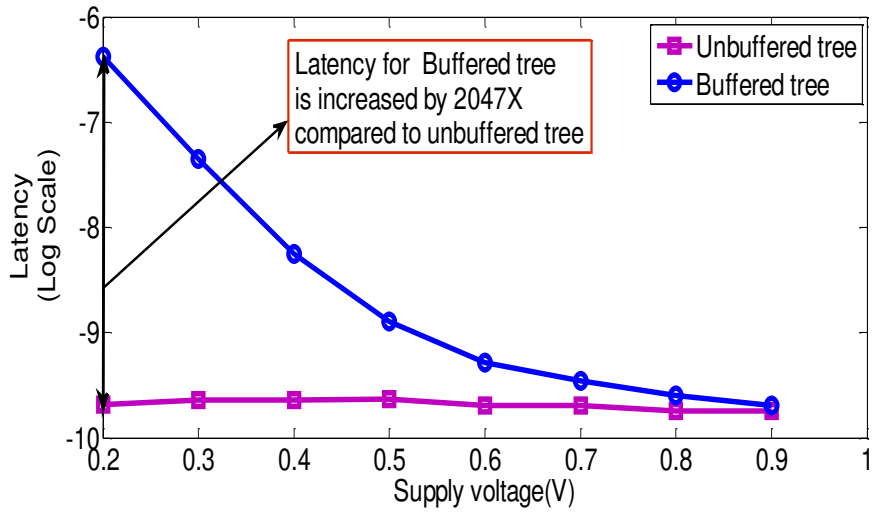


Figure 4.2: Impact of voltage scaling on latency

In super threshold region, the buffer resistance is very small, leading to comparable latency for buffered and un-buffered tree. But, as voltage is scaled to sub threshold region, the un-buffered tree proves to be superior since it exhibits lower latency. As indicated in Figure 4.2, the latency for clock system with buffered tree is increased by 2047 times compared to un-buffered tree at 0.2V.

Figure 4.3 shows impact of voltage scaling on power consumption for buffered and un-buffered tree. Reduction of supply voltage below threshold voltage results in exponential reduction in power consumption. In order to satisfy the slew constraint, a large driver is employed in un-buffered tree to switch the CDN whereas in buffered tree many small buffers are distributed in the CDN. The un-buffered tree consumes slightly more power than buffered tree in strong inversion region due to large driver whereas its power consumption becomes comparable to buffered tree in weak inversion region.

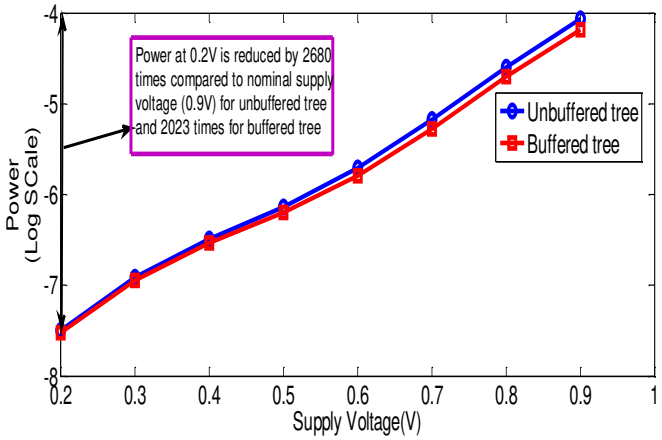


Figure 4.3: Impact of voltage scaling on power

Thus, the clock circuit with buffered and un-buffered tree shows comparable power consumption. The buffered tree shows an improvement of 14.7% in slew as compared to un- buffered tree in sub threshold regime. Latency for buffered tree is increased by 2047 times compared to un-buffered tree in sub threshold regime. Thus, latency is far better for un-buffered tree whereas slew is better for buffered tree in sub threshold region.

Moreover, though the latency affects the performance of system, it doesn't affect the functionality of system. What is major concern is the variation in latency which results in skew thereby leading to the malfunction. Therefore it is utmost important to do the variability analysis of clock system.

Monte Carlo simulations are performed considering ±10% variation in threshold voltage and ±10% variation in supply voltage [7] and ±20% variation in temperature. The results of process and PVT variability for clock system parameters for both buffered and un-buffered tree are observed.

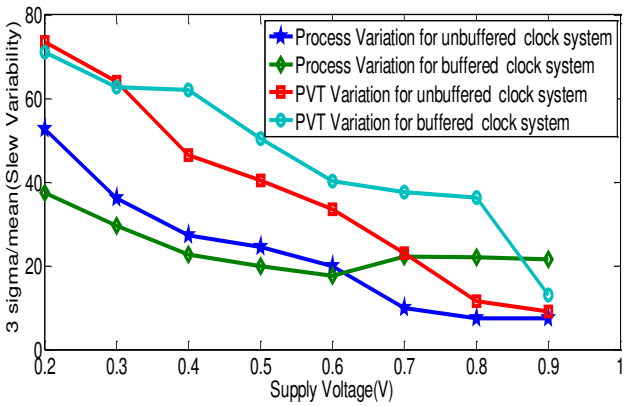


Figure 4.4: Impact of process variation and PVT variation on slew for buffered and un-buffered tree

Figure 4.4 shows the impact of process variation and PVT variation on slew for buffered and un-buffered tree. It shows that the slew increases exponentially as supply voltage is reduced. Variability in slew due to PVT variation for clock system with buffered as well as un-buffered tree is comparable at 0.2V and is increased drastically as compared to strong inversion region.

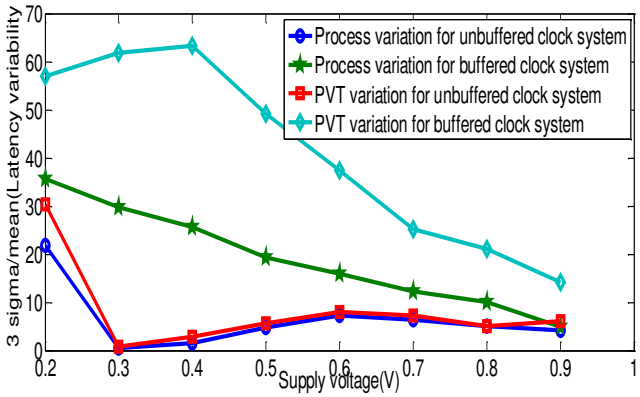


Figure 4.5: Impact of process variation and PVT variation on latency for buffered and un-buffered tree

Figure 4.5 shows the impact of process variation and PVT variation on latency for buffered and un-buffered tree. The variation in latency increases as supply voltage is reduced. The variability in latency due to process and PVT variation is increased for clock system with buffered tree compared to un-buffered tree by 38.99% and 46.83% respectively at 0.2V. The variation in latency of clock is thus extremely sensitive to the process and PVT variations in clock system with buffered tree.

Figure 4.6 shows impact of process variation and PVT variation on pulse width for buffered and un-buffered tree.

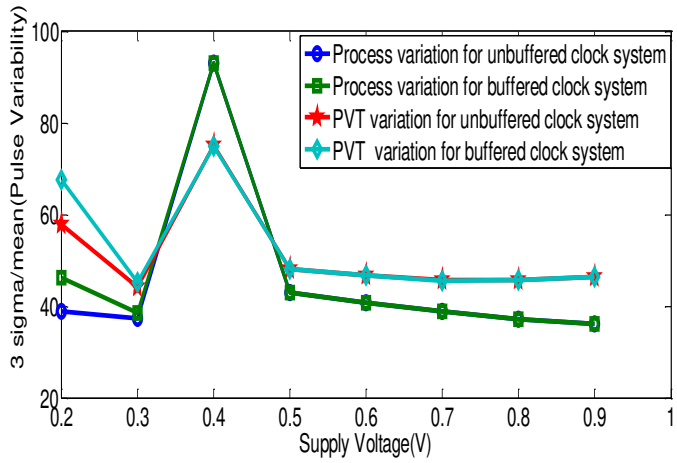


Figure 4.6: Impact of process variation and PVT variation on pulse width for buffered and un-buffered tree

In the simulation setup, with control voltage set at 200mV and initial conditions of 200mV, the impact of process and PVT variation on clock pulse width at the supply voltage ranging from 0.9V to 0.2V is observed. As supply voltage is reduced, the variability is increased. It is observed that pulse width variation for clock system with buffered and un-buffered tree overlap till supply voltage of 0.3V. Therefore, it is clear that clock generator (CSVCO) itself is dominating source for jitter. However, in deep sub threshold region the clock network also adds to the variability of pulse width. As evident from Figure 4.6, below 0.3V width of clock pulse will be further varied by CDN along with generator, as it travels from clock generator to the clocked elements through CDN. At 0.2V, the variation in pulse width, with process and PVT variation, for buffered tree is increased by 8.85% and 7.58% respectively compared to un-buffered tree.

In order to observe the impact of interconnect variation on clock system performance interconnect parameters; width (W), thickness (T) and spacing (S) are changed by ±10%. The corresponding RLC parameters of Cu interconnect are extracted from PTM tools.

Figure 4.7 shows the comparison of slew of buffered and un-buffered tree under nominal conditions and with width (W), thickness (T) and spacing (S) variation. A small deviation in slew is observed in super-threshold region under altered conditions compared to that of nominal, whereas this deviation is minimal in sub threshold for both buffered and un-buffered tree.

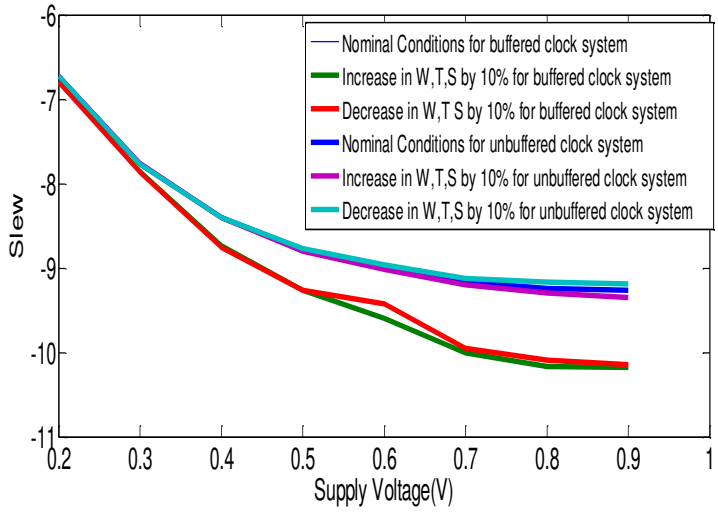


Figure 4.7: Comparison of slew of buffered and un-buffered tree under nominal conditions and with W, T and S variation

Figure 4.8 shows the comparison of latency of buffered and un-buffered tree under nominal conditions and with width (W), thickness (T), spacing (S) variation. The variation in latency is observed in the un-buffered tree under altered conditions. Since, with decrease in width and thickness, the resistance increases thereby increasing the latency by 27.87% at 0.2V. With buffered tree the variation is minimal.

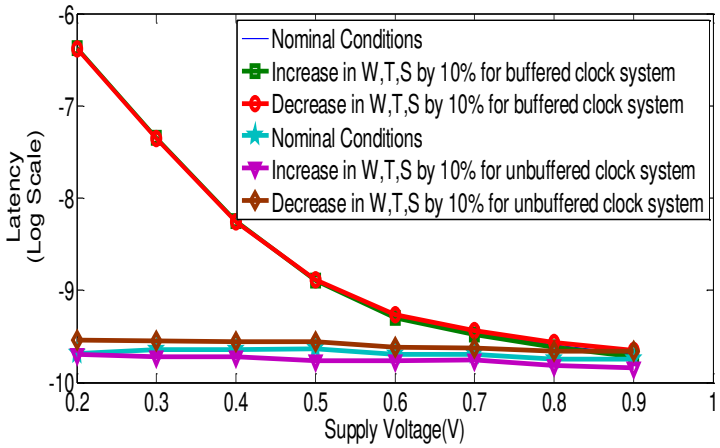


Figure 4.8: Comparison of latency of buffered and un-buffered tree under nominal conditions and with W, T and S variation

Figure 4.9 shows the comparison of slew of buffered and un-buffered tree with PVT variation and PVT + interconnects variation in width (W), thickness (T) and spacing (S). As evident from the results, the dominant source to bring about the variability in slew is PVT variation in devices.

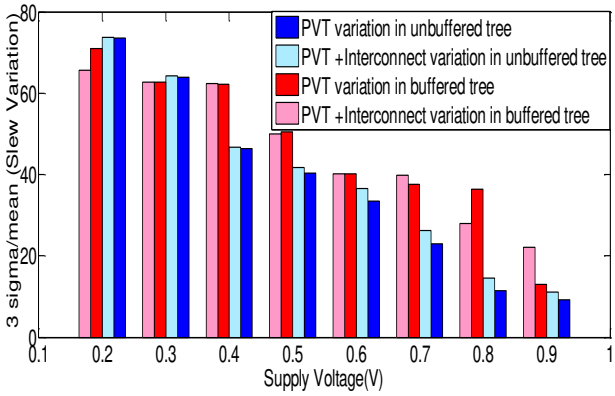


Figure 4.9: Comparison of slew variation of buffered and un-buffered tree with PVT variation and PVT +interconnect variation in W, T and S

Figure 4.10 depicts the comparison of variation in latency due to PVT variation in devices and variations in latency with PVT variations in devices along with interconnect variation. As shown the PVT variation in devices is the dominant source to bring about variability in latency as well.

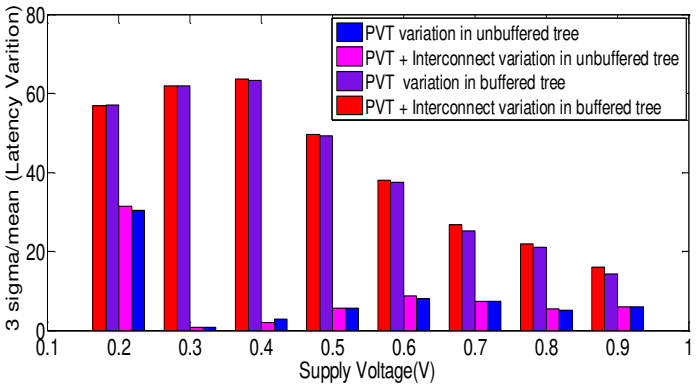


Figure 4.10: Comparison of latency variation of buffered and un buffered tree with PVT variation and PVT +interconnect variation in W, T and S

In previous part of this section it was seen that latency is better for clock system with un-buffered tree compared to the buffered tree in sub threshold regime. Higher latency degrades the performance and increases the power consumption [118]. Moreover, though the latency affects the performance of system, it doesn't threaten the functionality of system. The major concern is the variation in latency due to process, PVT and interconnects variation which results in skew thereby leading to malfunction. The Monte Carlo simulation results in this part of section shows that variability in latency and pulse width due to process and PVT variation is increased for clock system with buffered tree compared to un-buffered. Therefore, by comprehensively taking all the results into consideration, it can be concluded that clock system with un-buffered tree is a good option if its slew can be improved in sub threshold region. With the design methodology to reduce the slew as discussed in chapter 3, H tree design2 is obtained.

Figures 4.11-4.14 gives the comparison between design1 and design2. Design1 and 2 have been discussed in chapter 3 and shown by Figure 3.3 and 3.5 respectively.

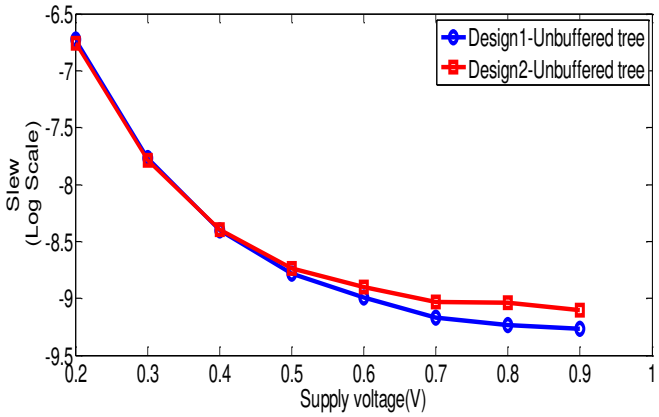


Figure 4.11: Comparison of slew for design1 and design2 for clock system with un-buffered tree

For un-buffered tree, with design2 the slew is degraded in strong inversion region but in weak inversion region, which is our area of interest, slew is improved by 7% compared to design1.

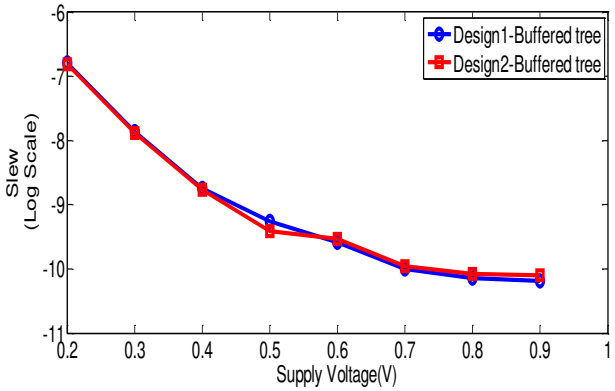


Figure 4.12: Comparison of slew for design1 and design2 for clock system with buffered tree

For buffered tree, slew for design2 is reduced by 5% at 0.2V compared to design1

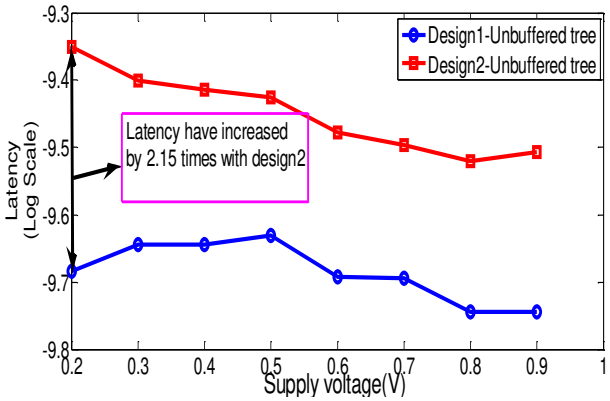


Figure 4.13: Comparison of latency for design1 and design2 for clock system with un-buffered tree

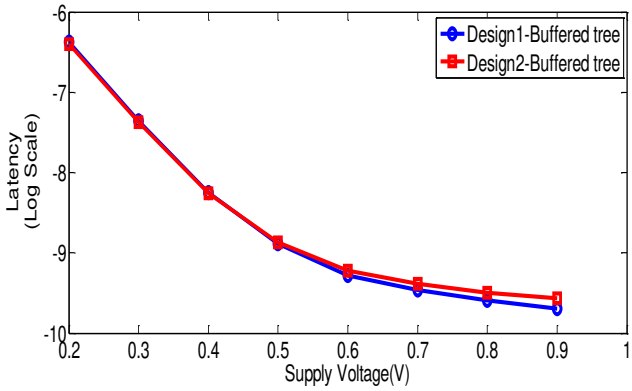


Figure 4.14: Comparison of latency for design1 and design2 for clock system with buffered tree

Latency has increased by almost 2 times for design2 compared to design1for un-buffered tree. For buffered tree, latency is increased by 4% with design2 compared to design1.

Figure 4.15 and 4.16 depict the comparison of variability in slew and latency of clock system with design1 and design2 CDN respectively. As seen from the results, variability in clock system with design2 is reduced as compared to design1.

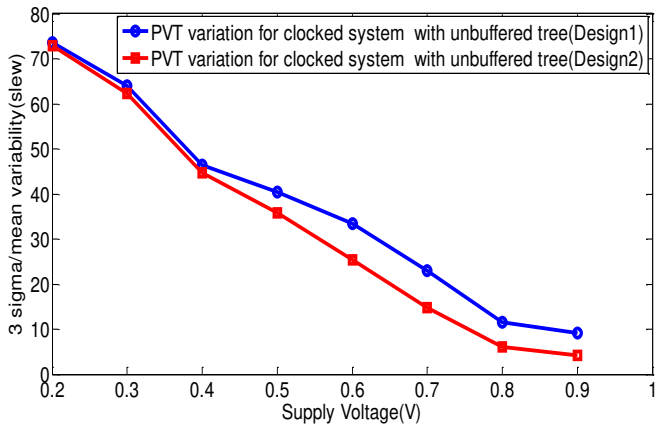


Figure 4.15: Comparison of slew variation for design1 and design2 for clock system with un-buffered tree

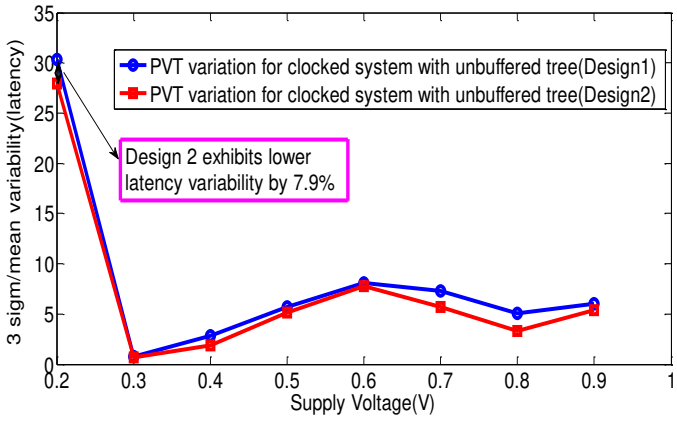


Figure 4.16: Comparison of latency variation for design1 and design2 for clock system with un-buffered tree

By comprehensively taking all the results into consideration, it can be concluded that clock system with un-buffered tree is a good option in sub threshold region. Though un-buffered tree exhibits better variability performance over buffered tree, still its sensitivity to process and environmental variation in sub threshold is quite high. Therefore techniques need to be devised to mitigate the impact of device variability to have stable clock system in sub threshold region to ensure the proper functionality of system. An attempt to improve slew of the sub threshold un-buffered CDN is made in this work by redesigning the tapered H tree CDN. The clock system

with proposed un-buffered CDN, design2, shows improvement in slew and exhibits less variability in sub threshold regime.

4.2 Performance and Variability Analysis of CMOS and Various Configurations of DTMOS Based CSVCO

A five stage CMOS based CSVCO and various configurations of DTMOS based CSVCO are designed using HSPICE at 32nm technology node using Predictive Technology Model (PTM) [90] and simulated at 0.3V supply voltage to observe the performance of CSVCO and DTCSVCO variants in sub threshold regime.

Figure 4.17 and Figure 4.18 show the time period of output pulse and slew of conventional CMOS CSVCO and various configurations of DTCSVCO respectively.

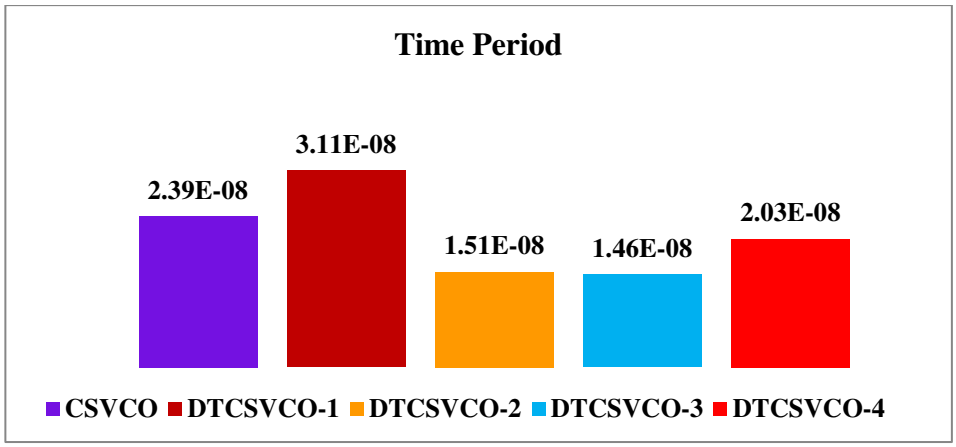


Figure 4.17: Time period comparison of CMOS CSVCO and DTCSVCO variants

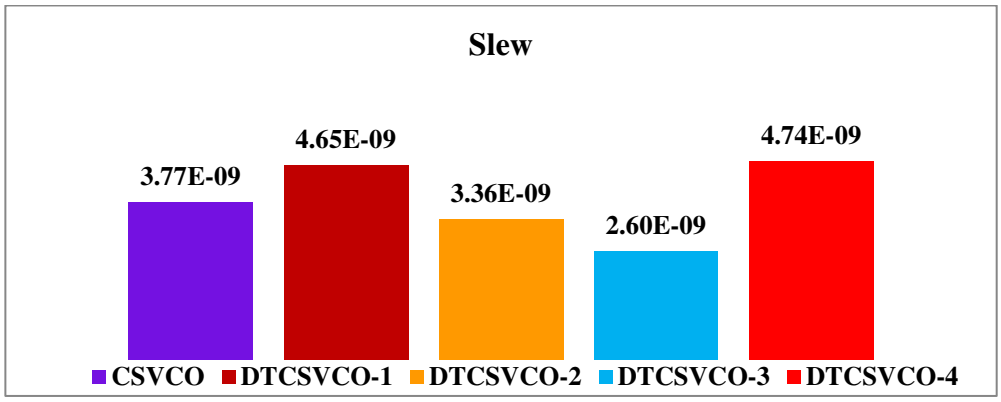


Figure 4.18: Slew parameter comparison of CMOS CSVCO and DTCSVCO variants

It is clear from the results that DTCSVCO-3 shows highest switching speed and least slew. But along with speed, energy efficiency of various CSVCO configurations

also needs to be observed and PDP is one of measures to determine energy efficiency of a circuit. Figure 4.19 shows the PDP of CSVCO and DTCSVCO variants.

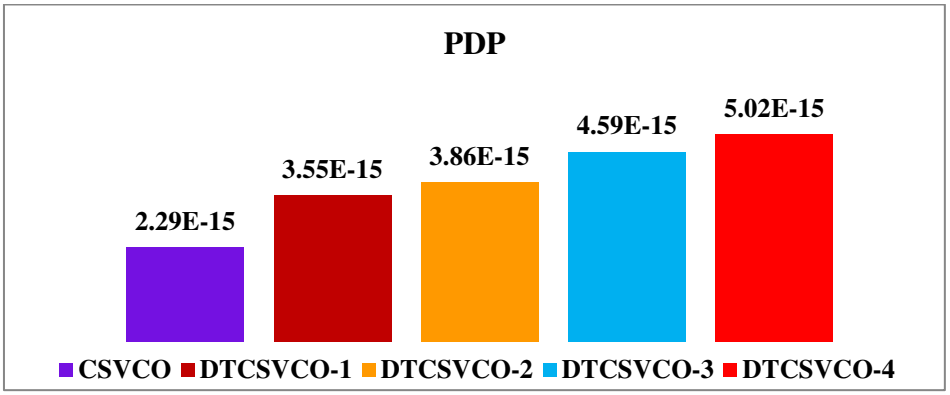


Figure 4.19: PDP Comparison of CMOS CSVCO and DTCSVCO variants

PDP of conventional CMOS CSVCO is least, but its speed is very low. PDP of DTCSVCO-1 and DTCSVCO-2 are comparable, but the switching speed of DTCSVCO-2 is more than DTCSVCO-1 and conventional CSVCO. DTCSVO-2 shows an increased in switching speed by 51.44% and 36.88% respectively as compared to DTCSVCO-1 and conventional CSVCO respectively. DTCSVCO-2 exhibits better PDP than DTCSVCO-3 and 4. This is because the increased gate capacitance in DTCSVCO-3 and DTCSVCO-4 outperforms improvement in drive current thereby increasing their PDP. Thus DTCSVCO-2 gives optimum performance producing the output waveform of 66.22 MHz and power consumption of 0.257µW at 0.3V.

Monte Carlo simulations are performed considering ±10% variation in V_{th} [7]. 3σ/µ variability of time period using Monte Carlo analysis is depicted in Figure 4.20.

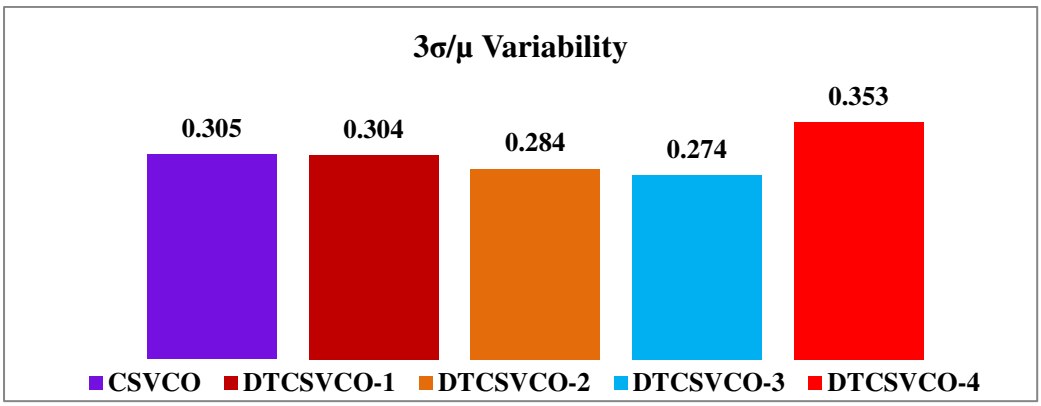


Figure 4.20: Impact of process variation on time period of CMOS CSVCO and DTCSVCO variants

Figure 4.20 clearly indicates that DTCSVCO-2 and DTCSVCO-3 exhibits better robustness compared to other configuration. To investigate the sensitivity of DTCSVCO-2 against temperature variation, temperature is varied from 10° C to 120° C and time period variability is observe. Figure 4.21 shows the impact of temperature variation on time period of DTCSVCO-2 at different process corners. It is clear that the time period of DTCSVCO-2 is stable over wide temperature range and this result is consistent at different process corner as well. Figure 4.21 also demonstrates time period variability of conventional CSVCO. The DTCSVCO-2 exhibits lower variability to temperature variation by almost 45.63% at TT corner compared to conventional CSVCO.

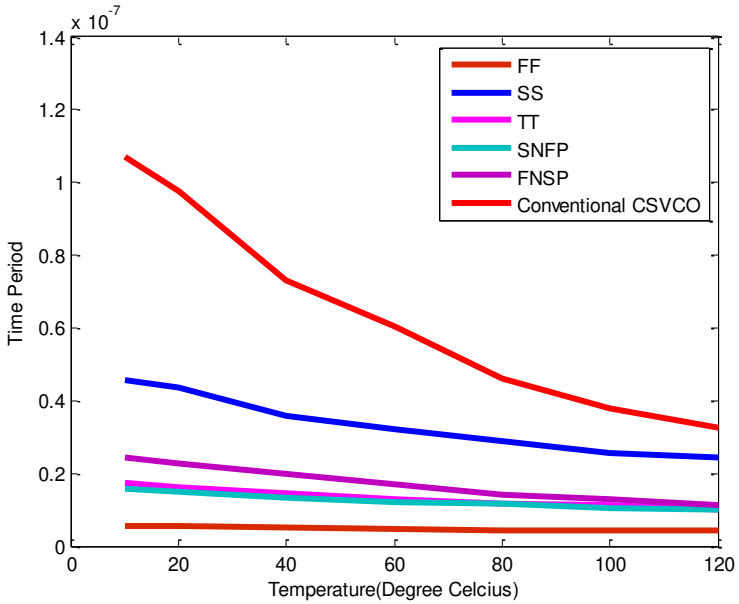


Figure 4.21: Impact of temperature variation on time period of DTCSVCO-2 at different process corners and conventional CSVCO

The temperature error of proposed DTCSVCO-2 is 3423ppm/°C which is better compared to conventional CSVCO which exhibits temperature error of 6348ppm/°C. In proposed DTCSVCO no temperature sensor and stabilization circuits are used. As a result of self biasing, the DTMOS transistor operates at the onset of moderate inversion region where, the current is not exponentially dependent on temperature and is therefore inherently less sensitive to temperature variations, giving simple and low power robust clock circuit. Thus from the comprehensive result analysis of variability, performance and PDP parameter of various CSVCO configurations, it is clear that DTCSVCO-2 configuration is an energy efficient, enhanced speed and robust VCO.

4.3 Performance Analysis of Proposed Thermally Aware Clock Generator Circuit

To investigate the effect of temperature variation in super threshold and sub threshold regime, a five stage voltage controlled ring oscillator is designed at 32 nm technology node using PTM and simulated in HSPICE for the super threshold (supply voltage=0.9V) and the sub threshold (supply voltage=0.3V) region. Figure 4.22 and 4.23 depicts the simulation result of variation of time period of output pulse of conventional CSVCO with temperature at 0.9V and 0.3V respectively.

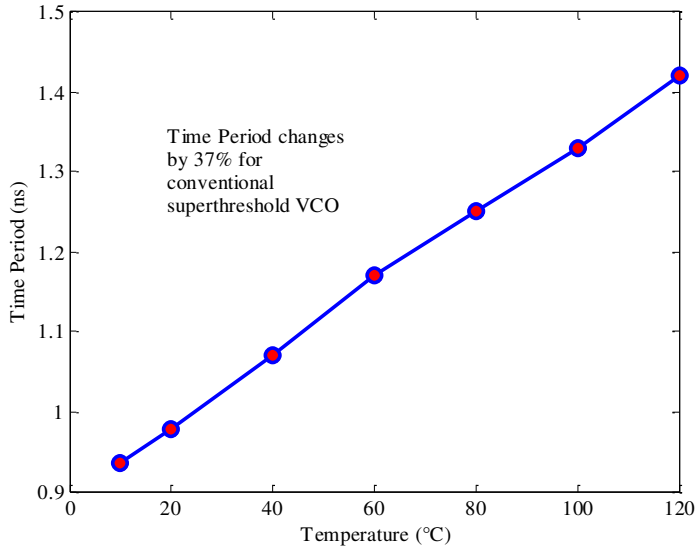


Figure 4.22: Time period versus temperature for conventional CSVCO at 0.9V supply voltage (super threshold)

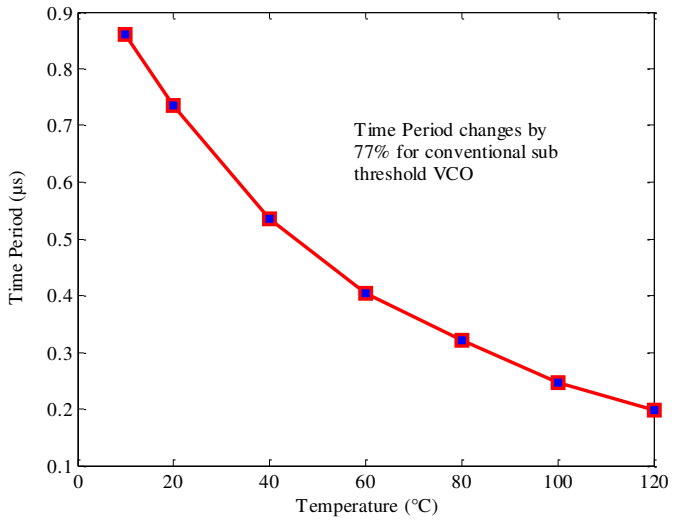


Figure 4.23: Time period versus temperature for conventional CSVCO at 0.3V supply voltage (sub threshold)

It is observed that the sub threshold ring oscillator is highly sensitive to temperature variation. The conventional CMOS CSVCO shows 37 % deviation in clock period with temperature variation from 10 °C to 120 °C in super threshold region, whereas 77% variation in time period is observed in sub threshold region. Thus, this exponential dependency of the time period on temperature in sub threshold regime is a major concern and therefore calls for design of thermally aware VCO for reliable operation.

To reduce the effect of temperature, a control circuit is designed in this work. The control circuit incorporates temperature monitoring circuit and control voltage generator circuit. In order to investigate the optimum operating supply voltage, the proposed compensated VCO is designed at 32 nm technology node using PTM and simulated with the varying supply voltages within the sub threshold regime. The temperature coefficient for delay and corresponding power consumption for the different supply voltages are depicted in Figure 4.24.

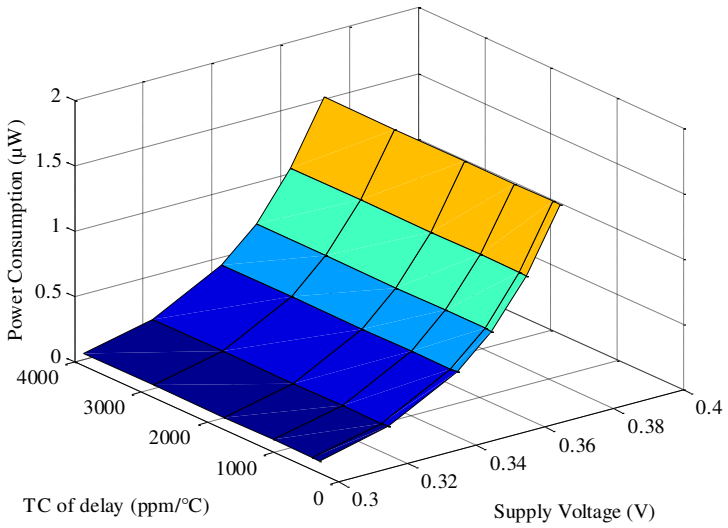


Figure 4.24: Variation in temperature coefficient of delay and power consumption at different supply voltages in sub threshold

Figure 4.24 indicates that as the supply voltage is increased, the temperature coefficient is reduced whereas the power consumption is correspondingly increased. At the supply voltage of 0.37V, which is still 120mV below the threshold voltage, the minimum temperature coefficient of 290ppm/°C is obtained over a wide temperature variation of 10° C to 120° C. The power consumption of the proposed VCO is 1.56µW at room temperature. For the supply voltage greater than 0.37V, an increase

in the temperature coefficient and the power consumption is observed. Thus, the 0.37V supply voltage can be considered as an optimal choice.

Figure 4.25 shows the plot of output voltage against temperature variation for temperature monitoring circuit. It is found that the output voltage of temperature monitoring circuit (V_{temp}) increases linearly with the increase in temperature. And hence V_{temp} can be used as the temperature monitoring parameter. Thus, the increase in temperature results in the increase in the output voltage of temperature monitoring circuit which in turn decreases the output of the control circuit. Figure 4.26 shows that the output of the control circuit decreases linearly with the increase in temperature.

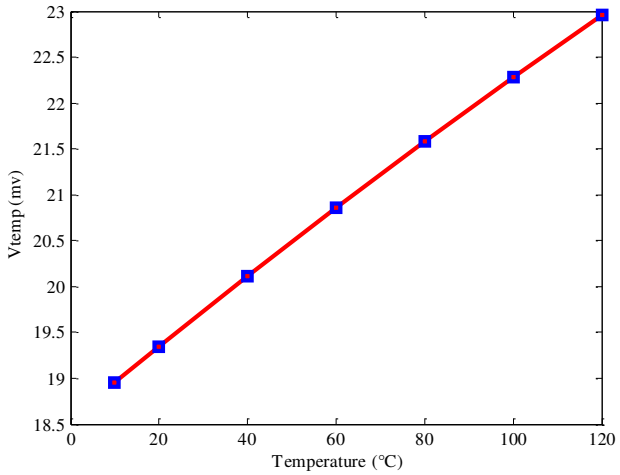


Figure 4.25: Vtemp as a function of temperature

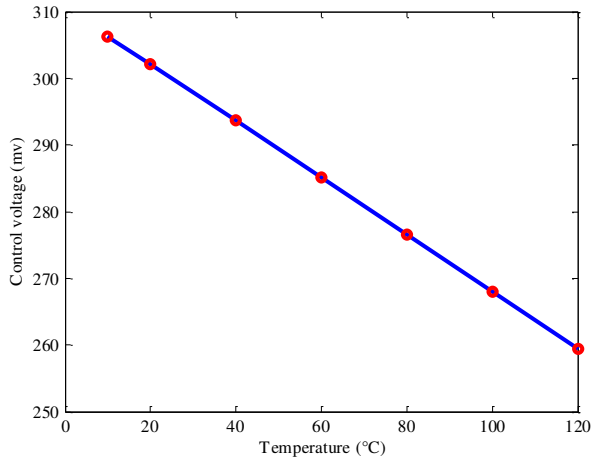


Figure 4.26: Control voltage as a function of temperature

Since the time period of the clock is a function of temperature, by providing the adaptive control voltage at the control voltage terminal of the CSVCO, the temperature effect on the time period of the clock pulse is mitigated.

4.3.1 Analysis of Conventional and Proposed VCO

Figure 4.27 demonstrates the behavior of the proposed VCO and the conventional VCO with the temperature variation at 0.37 V supply voltage. It clearly shows that the time period variation of the compensated VCO is reduced significantly over a wide range of temperature as compared to the conventional VCO.

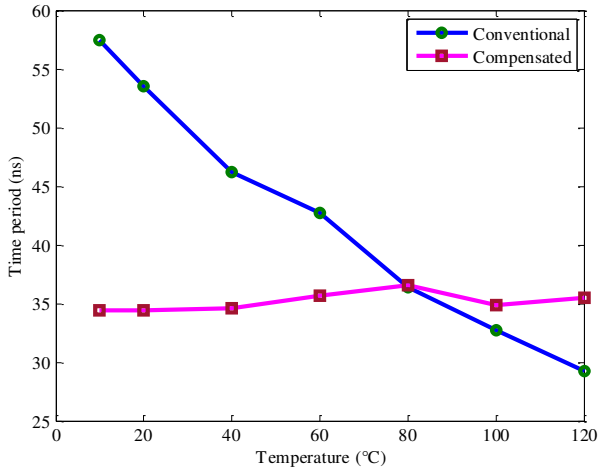


Figure 4.27: Time period as a function of temperature

The conventional VCO shows the delay variation with temperature coefficient of 4474ppm/°C and consumes 1.06µW power with 0.37V supply voltage. On the other hand, the proposed VCO shows the delay variation with temperature coefficient of 290ppm/°C and power consumption of 1.49µW with 0.37V supply voltage. The proposed VCO exhibits 49.2% and 82.79% less variation in time period of output pulse and power consumption respectively compared to the conventional VCO, over a wide range of temperature variation from 10° C to 120° C.

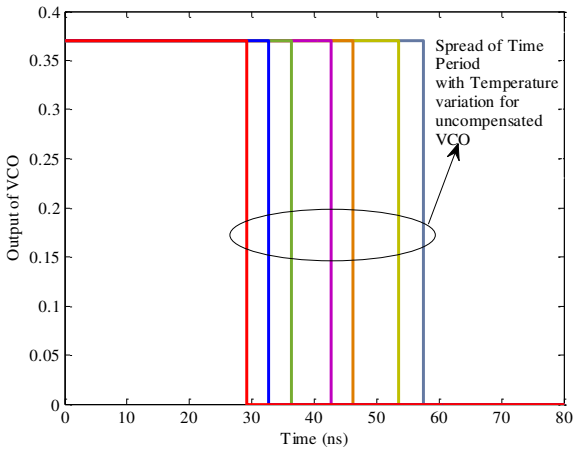


Figure 4.28: Clock pulse width variation with temperature for uncompensated VCO

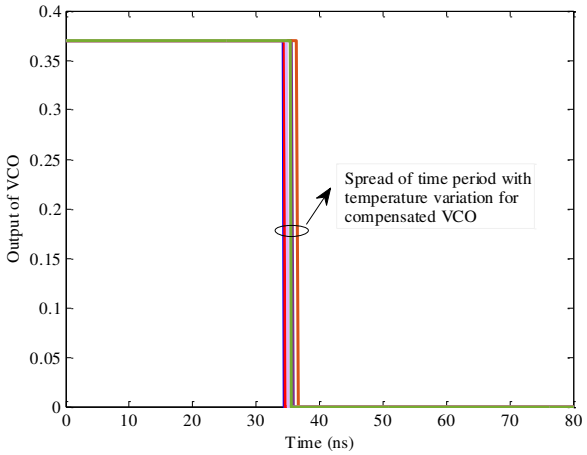


Figure 4.29: Clock pulse width variation with temperature for compensated VCO

Figure 4.28 and 4.29 show the variation in clock pulse width with the temperature variation for the uncompensated and the compensated VCO respectively.

Power consumption of the proposed compensated VCO is investigated and compared with the conventional sub threshold VCO. Figure 4.30 demonstrates the power consumption of the compensated VCO and the conventional sub threshold VCO.

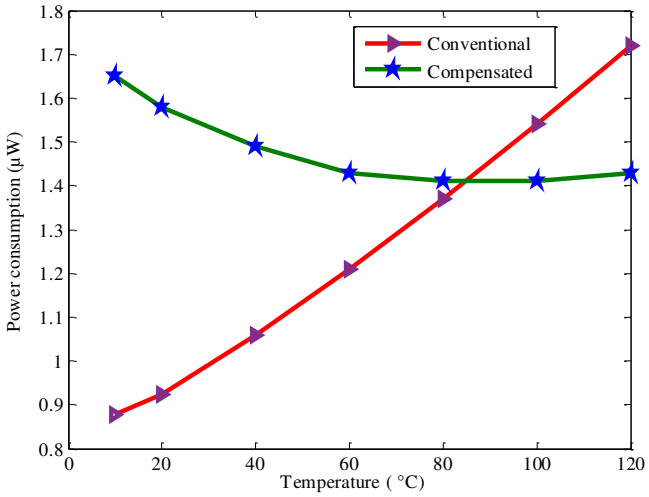


Figure 4.30: Power consumption of compensated and conventional sub threshold VCO

Since all the transistors in the control circuit are operated in the sub threshold region, there is a small increase in the power consumption. With the small increase in overall power consumption, the variation in the time period of the clock pulse is controlled.

4.3.2 Comparison of Proposed System with Published Work

Table 4.1 shows the comparison of the proposed system with the published work. Thus, the proposed compensated CSVCO proves to be a power efficient VCO with reduced temperature sensitivity, which is a major demand in applications like pace maker, RFID tags, wrist watches, biomedical sensors and wireless sensors.

Table 4.1: Comparison of proposed system with the published work

	[119]	**[64]**	**[65]**	**[62]**	**[120]**	**[121]**	**Proposed**
Process	0.5 um	0.18 um	0.35 um	90 nm	0.35 um	180 nm	32nm
Supply voltage (V)	3	1.25	1	0.3	3.3	1.8	0.37
Frequency (MHz)	12.8	6-24	0.08	235	4	4000	30
Power (uW)	133	1.12	1.14	7	234.72	11060	1.5
Temp. range (°C)	-40 to 125	-40 to 85	0 to 80	0 to 125	-25 to 100	0 to 120	10 to 120
Temp. error (ppm /°C)	3030	N/A	842	89.1	986	108	290

4.4 Performance Comparison of Various Configurations of H-tree CDN with Hybrid Buffers

Figure 4.31 shows the slew of clock system with tapered buffered and un-buffered tree for super threshold, near threshold and sub threshold region.

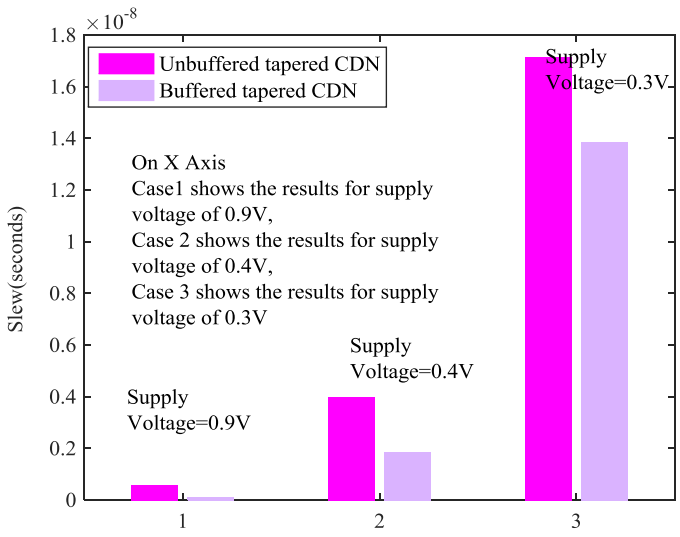


Figure 4.31: Slew of clock system with buffered and un-buffered tree

From Figure 4.31, it is clear that slew of the clock system with un-buffered tree is comparatively more than buffered tree. As revealed from the results in section 4.1, the clock system with un-buffered tree exhibit better latency and robustness in sub threshold regime. Therefore techniques need to be explored to improve the slew of un-buffered tree in sub threshold regime.

The comparison of optimized uniform un-buffered H tree, tapered un-buffered and tapered buffered H- tree is depicted in Figure 4.32.

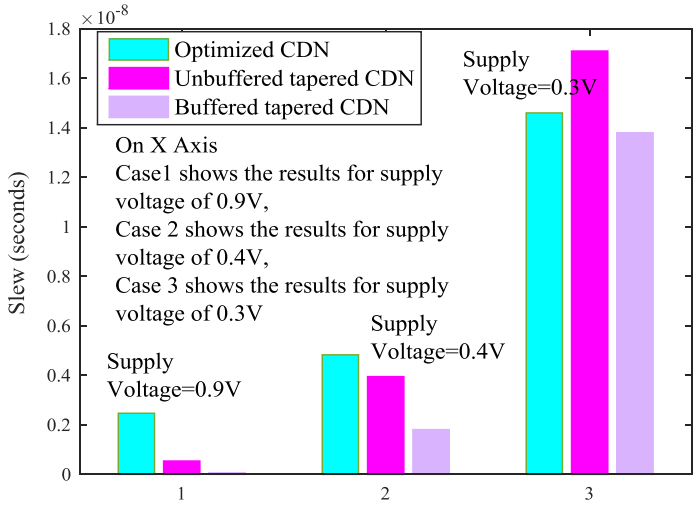


Figure 4.32: Comparison of tapered and optimized H tree slew performance

Tapered H-tree shows better results compared to optimized uniform H-tree in super threshold and near threshold region for both buffered and un-buffered CDN. However, in sub threshold region, un-buffered optimized uniform H-tree exhibits better results compared to tapered un-buffered tree. The optimized uniform un-buffered H tree exhibits better slew compared to tapered un-buffered H tree by 14.61%. However, still buffered tapered tree is better than optimized uniform H un-buffered tree by 5.47% in sub threshold region.

Thus, even though un-buffered tree can be an appropriate choice from better skew and variability aspect, it exhibits degraded slew compared to buffered tree. Therefore, a strategy need to be devised which will take the advantage of un-buffered tree as better stability and better skew and seek the advantage of buffered tree as having better slew.

Figure 4.33 shows the performance comparison of optimized CDN with buffer at sink nodes in various configurations as discussed in chapter 3.

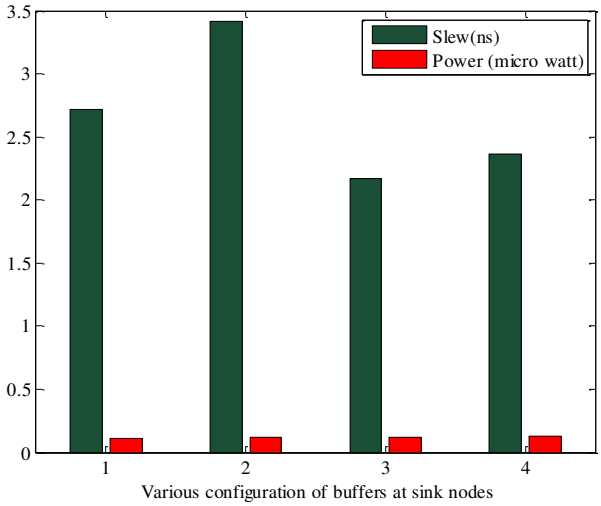


Figure 4.33: Performance comparison of optimized CDN with various configurations of buffer in last stage

Configuration 1 exhibit increased slew because of degraded performance of conventional sub threshold CMOS. Configuration 2 has DTMOS buffer in the last stage and it exhibits largest slew. Configuration 4 exhibits largest power consumption and degraded slew compared to configuration 3. Configuration 3 exhibits improved slew compared to all other configurations.

Figure 4.34 illustrates the slew comparison obtained by simulating the clock circuit with conventional tapered un-buffered H-tree and clock circuit with optimized uniform H- tree with configuration 3 for clock network designed for die size of 1mmx1mm (Case 1 in Figure 4.34) , 2mmx2mm (Case 2 in Figure 4.34) and 3.5mmx3.5mm (Case 3 in Figure 4.34) chip at 0.3V.

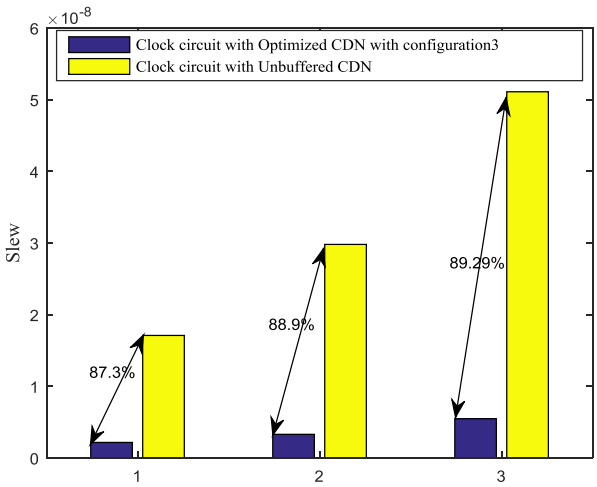


Figure 4.34: Slew comparison of clock circuit with conventional tapered un- buffered CDN and with optimized uniform CDN with configuration3

Figure 4.35 illustrates the power consumption comparison of clock circuit with conventional tapered un-buffered H tree and clock circuit with optimized uniform H-tree with configuration 3 for clock network designed for die size of 1mmx1mm (Case 1 in Figure 4.35) , 2mmx2mm (Case 2 in Figure 4.35) and 3.5mmx3.5mm (Case 3 in Figure 4.35) chip at 0.3V.

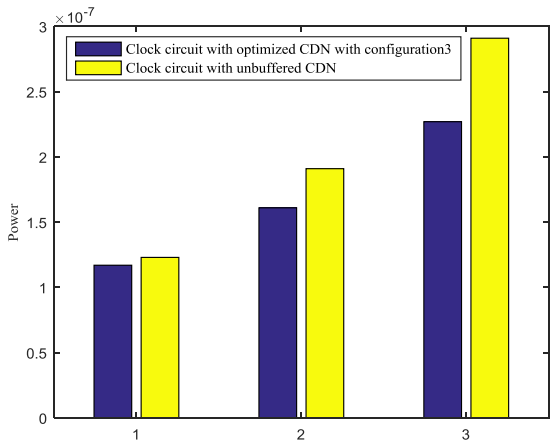


Figure 4.35: Power consumption comparison of clock circuit with conventional tapered un-buffered CDN and with optimized uniform CDN with configuration3

The simulation results in Figure 4.34 and 4.35 clearly indicate that improved slew is obtained by optimized uniform CDN with configuration 3 with added advantage of reduced power consumption. The slew for optimized uniform H-tree with configuration 3 is also improved compared to tapered buffered H–tree by 84.27% for clock network designed for die size of 1mmx1mm at 0.3 supply voltage. Thus, uniform optimized H tree CDN with configuration 3 at last stage is a good solution and therefore can be proposed for sub threshold clock circuit.

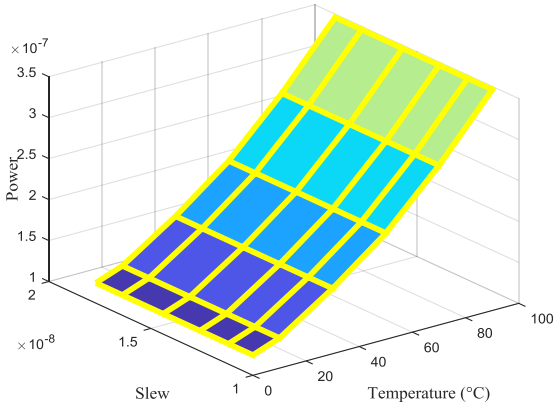


Figure 4.36: Impact of temperature variation on slew and power for clock circuit with tapered un-buffered CDN

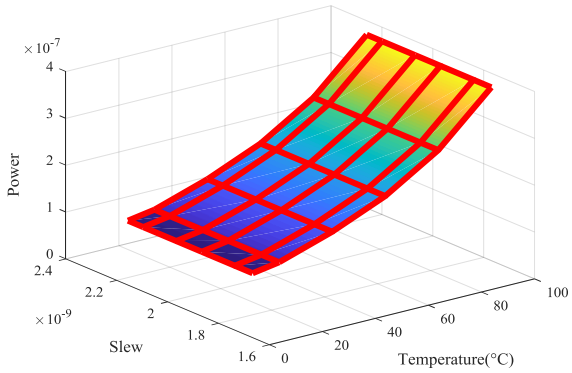


Figure 4.37: Impact of temperature variation on slew and power for clock circuit with proposed CDN

Figure 4.36 and 4.37 illustrates the impact of temperature variation on slew and power for conventional tapered un-buffered CDN and proposed CDN respectively. The proposed CDN exhibits 18.8% less variability compared to tapered un-buffered CDN with temperature variation from 10 °C to 100 °C.

In order to investigate the impact of process variation, ±20% variation in threshold voltage is considered. The results of 3σ Monte Carlo simulation are depicted in Figure 4.38 and 4.39 for tapered un-buffered and proposed CDN respectively.

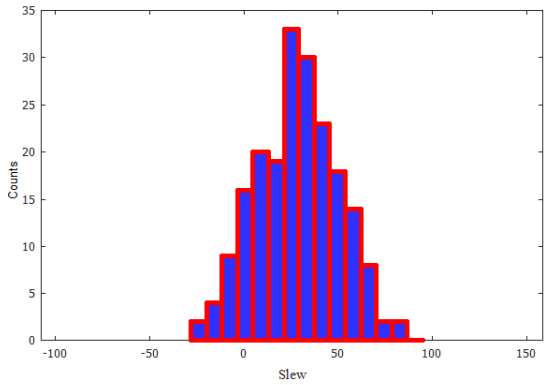


Figure 4.38: Impact of process variation on slew for clock circuit with tapered un-buffered CDN

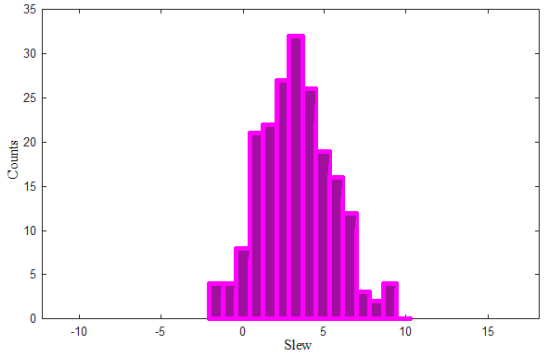


Figure 4.39: Impact of process variation on slew for clock circuit with proposed CDN

The result indicates 11% reduction in slew spread with proposed CDN compared to un-buffered CDN.

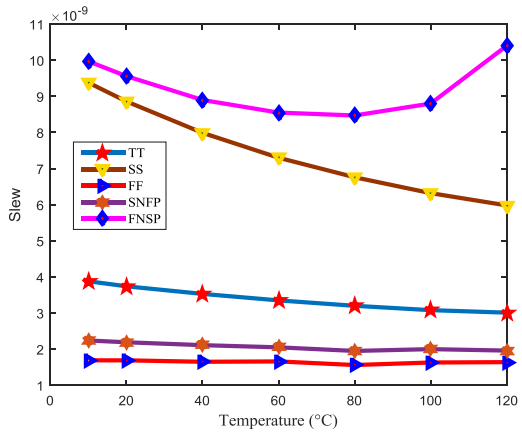


Figure 4.40: Slew as a function of temperature at different process corners

The effect of process and temperature can be collectively analyzed by simulating the circuit at different process corner. Figure 4.40 depicts slew as function of temperature at different process corner. The results showcased in Figure 4.40 indicate that slew with proposed CDN shows good consistency for TT, FF and FNSP corners as well.

4.4.1 Performance Comparison of CMOS Clock System and Hybrid DTMOS-CMOS Clock System

In section 4.2, various configurations of DTMOS based CSVCO are explored. The results indicate that the hybrid DTCSVCO-2 exhibits better performance compared to all other configurations of DTMOS based VCO as well as CMOS based VCO. This sub section explores the performance of two clock systems enumerated below:

1. Clock System with CMOS CSVCO clock generator and proposed H tree CDN with configuration 3 - CMOS Clock System.
2. Clock System with Hybrid DTCSVCO-2 clock generator and proposed H tree CDN with configuration 3- Hybrid Clock System.

The results obtained while investigating the challenges in design of ULP clock circuit indicated that ULP clock system with buffered CDN exhibit better slew whereas ULP clock system with un-buffered CDN exhibit better latency. For better performance, both slew and latency must be minimized. In order to investigate the performance of the CMOS and DTMOS based VCO, a new performance parameter, Slew Latency Product (SLP) is considered in this work. For better performance SLP must be less.

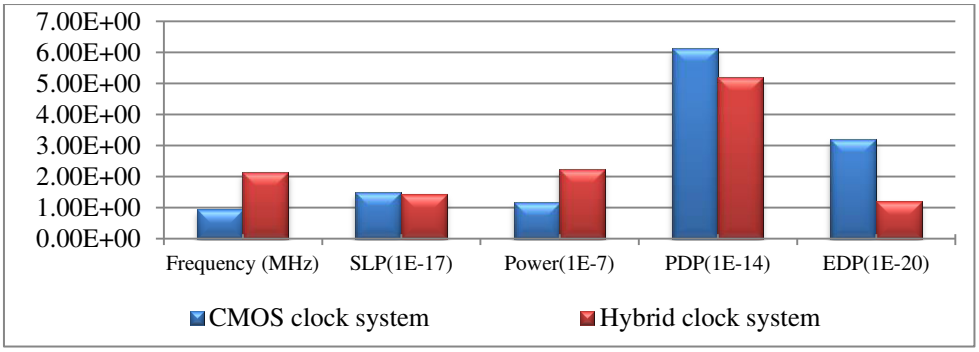


Figure 4.41: Performance Comparison of CMOS and Hybrid clock system

Figure 4.41 shows the performance comparison of CMOS and Hybrid clock system. As indicated by Figure 4.41, hybrid clock system exhibit higher frequency and lower SLP, but this comes at the cost of increased power consumption. However PDP and EDP exhibited by hybrid clock system are better compared to CMOS clock system. Thus hybrid clock system exhibit better performance compared to CMOS clock system.

4.5 Performance Analysis of DG Fin-FET Based Clock Generator Circuits

This section presents design of DG FinFET based ULP sub threshold CSVCO circuit. Performance comparison of CMOS and DG FinFET based CSVCO is done in this section. Furthermore, seven different configurations of five stages CSVCO have been explored to investigate the optimal configuration for sub threshold applications.

4.5.1 Performance Comparison of Bulk CMOS and DG Fin-FET Based VCO

CMOS based and SG DG Fin-FET based CSVCO circuit, shown in Figure 3.6 and 3.13 respectively in chapter 3, are designed in HSPICE at 32 nm technology nodes using PTM and simulated with supply voltage of 150mV.

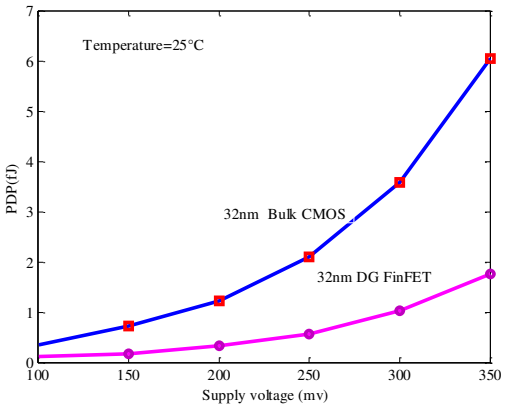


Figure 4.42: PDP comparison of Bulk CMOS and DG FinFET CSVCO with variation in supply voltage

PDP of Bulk CMOS CSVCO and DG Fin-FET CSVCO is observed and its variation with supply voltage is plotted in Figure 4.42. The SG DG Fin-FET improves the drive current by two times [122] and hence PDP for DG Fin-FET CSVCO is improved drastically. PDP of DG Fin-FET CSVCO is improved by 77% compared to Bulk CMOS CSVCO at supply voltage of 150mV at room temperature.

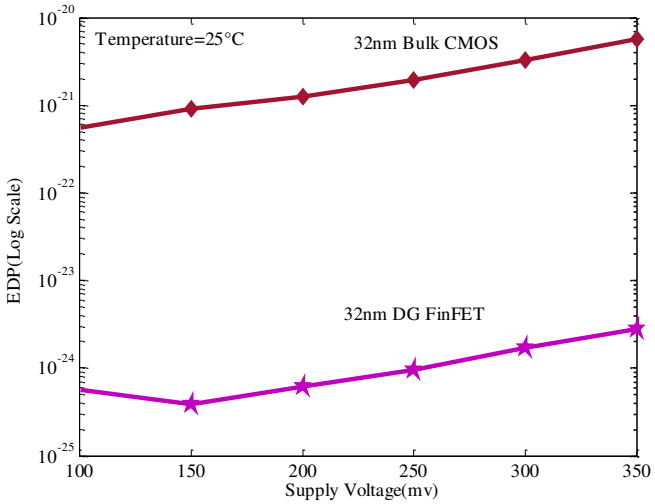


Figure 4.43: EDP comparison of Bulk CMOS and DG FinFET CSVCO with variation in supply voltage.

Energy Delay Product (EDP) of CSVCO with Bulk CMOS and DG Fin-FET is explored and plotted as shown in Figure 4.43. EDP of DG Fin-FET CSVCO is lesser by almost 2300 times, than Bulk CMOS CSVCO.

To observe the impact of device process variability on CMOS based and DG FinFET based CSVCO output pulse width and EDP, Monte Carlo simulations are performed by considering ±10 % variation in V_{th}. The results of variation in pulse width for CMOS based and DG FinFET based CSVCO are depicted in Figure 4.44 and 4.45 respectively.

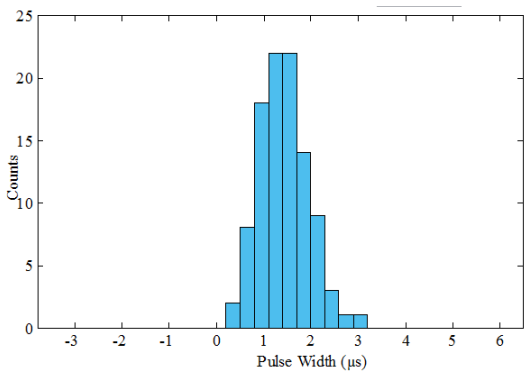


Figure 4.44: PDF for Bulk CMOS CSVCO

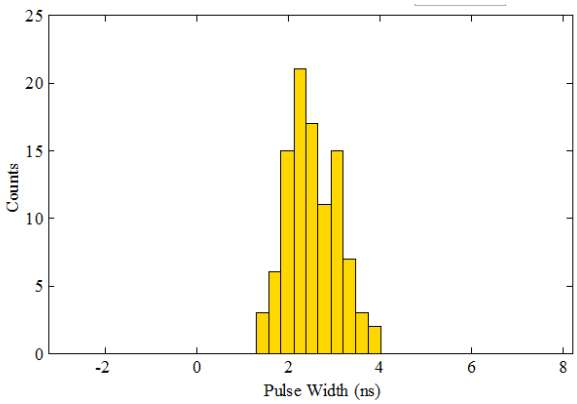


Figure 4.45: PDF for DG FinFET CSVCO

The spread in pulse width is reduced in DG FinFET CSVCO compared to Bulk CMOS CSVCO exhibiting the improved robustness in DG FinFET CSVCO.

Figure 4.46 and 4.47 show the spread in EDP in bulk CMOS CSVCO and DG FinFET CSVCO respectively.

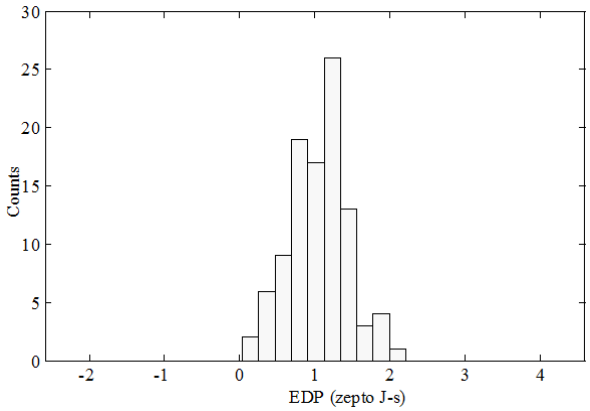


Figure 4.46: PDF for Bulk CMOS CSVCO

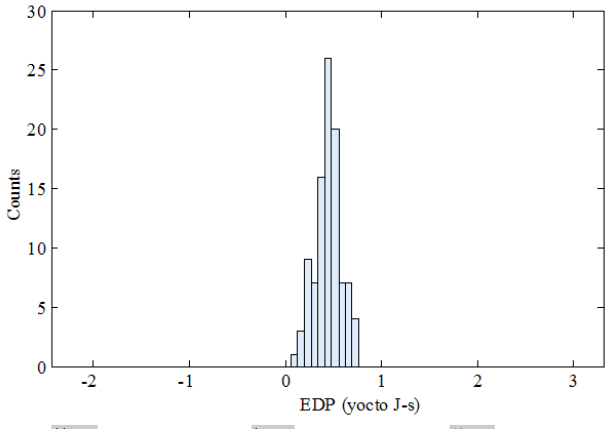


Figure 4.47: PDF for Bulk DG FinFET

The spread in EDP is reduced in DG FinFET CSVCO compared to bulk CMOS CSVCO. Thus, the results show that the DG FinFET based CSVCO gives improved

performance as well as robustness compared to bulk CMOS CSVCO in sub threshold region.

4.5.2 Performance Analysis of Different Configurations of DG Fin-FET VCO Circuits

Seven configurations of DG Fin-FET based VCO, as discussed in chapter 3, are designed using HSPICE at 32 nm technology node using PTM and are simulated at 150mV supply voltage to investigate their performance in sub threshold regime. Table 4.2 shows the performance parameters of various DG FinFET CSVCO configurations

Table 4.2: Comparison of performance parameters of DG FinFET based CSVCO configurations

	CSVCO Configurations						
	SG	**IG**	**Hybrid**	**Hybrid reverse**	**pignsg**	**psgnig**	**MIGFET**
Pulse width(ns)	2.36	8.03	2.92	10.2	2.75	9.18	1.17
Frequency(MHz)	212	62.2	171	49	182	54.5	426
Power(nW)	70.3	21.2	43.9	33	45.4	27.6	127
PDP (J)	1.66E-16	1.70E-16	1.28E-16	3.37E-16	1.25E-16	2.54E-16	1.49E-16
EDP(J-s)	3.91E-25	1.36E-24	3.74E-25	3.44E-24	3.43E-25	2.33E-24	1.75E-25

It is observed that Hybrid CSVCO exhibits better PDP. It improves by 23% compared to SG and 25% compared to IG. And EDP is also improved by 4% compared to SG and 72.5% compared to IG. In Hybrid reverse configuration of CSVCO the charging capacitance increases and charging current reduces and hence hampers the performance drastically compared to all other configurations.

It is also observed that the Pignsg CSVCO exhibits better performance than Hybrid CSVCO because of enhanced drive current and reduction on capacitance. PDP and EDP of pignsg CSVCO is improved compared to Hybrid CSVCO by 2.34% and 8.3% respectively.

The overall performance of Psgnig CSVCO is degraded as compared to SG, IG, hybrid and pignsg CSVCO because of reduction in drive current and increase in capacitance.

PDP of pignsg CSVCO is better compared to MIGFET CSVCO by 16%. This is because of the increased capacitance in MIGFET configuration. But MIGFET CSVCO has better output frequency and EDP as compared to other CSVCO.

Figure 4.48, 4.49 and 4.50 shows the variation in pulse width, PDP and EDP respectively for SG, IG, Hybrid, Hybrid Reverse, pignsg, psgnig, and MIGFET CSVCO configurations with variation in front and back gate oxide.

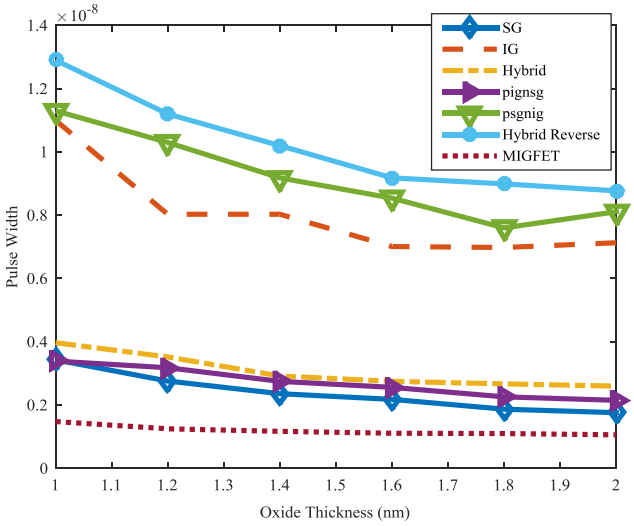


Figure4.48: Variation of pulse width of DG FinFET CSVCO variants with oxide thickness for sub threshold operation

It is observed that SG CSVCO exhibits highest pulse variability of 48.6% as compared to other configurations. IG, Hybrid, Hybrid reverse and pignsg CSVCO show less pulse width variability compared to SG CSVCO by 13.42%, 14% 16.6% and 12% respectively.

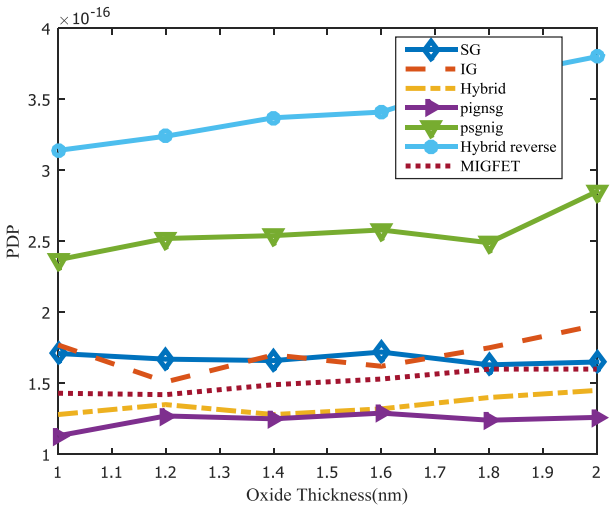


Figure 4.49: Variation of PDP of DG FinFET CSVCO variants with oxide thickness for sub threshold operation

The variation of PDP with oxide thickness is shown in Figure 4.49. MIGFET, Hybrid and pignsg CSVCO show almost same variation in PDP with oxide thickness variation.

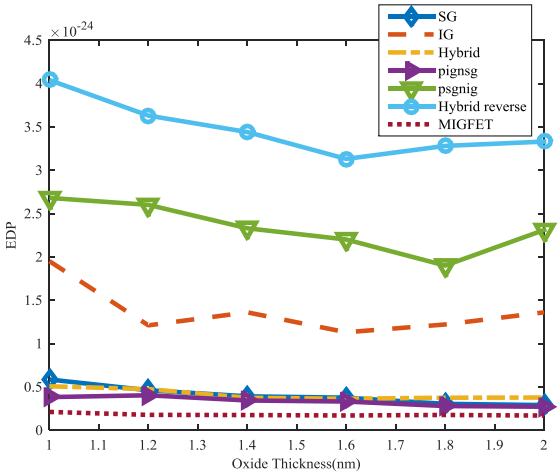


Figure 4.50: EDP variation sensitivity of DG FinFET CSVCO variants with oxide thickness for sub threshold operation

EDP variability in MIGFET CSVCO with oxide thickness variation is reduced by 30.5%, 5.7% and 9.9% compared to SG, Hybrid and pignsg CSVCO respectively as indicated by Figure 4.50.

Figure 4.51, 4.52 and 4.53 shows the variation in pulse width, PDP and EDP respectively for SG, IG, Hybrid, Hybrid Reverse, pignsg, psgnig, and MIGFET CSVCO configurations with variation in tsi.

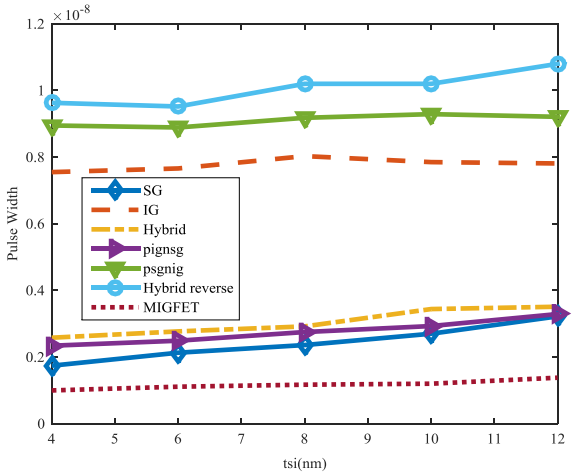


Figure 4.51: The pulse width variation sensitivity of DG FinFET CSVCO variants with t_{si} for sub threshold operation

SG CSVCO exhibits highest pulse width variability of 46%. In IG configuration only 3.32% variability in pulse width is observed. Hybrid CSVCO exhibits lesser pulse variability with t_{si} variation compared to SG CSVCO. Hybrid reverse CSVCO

exhibits lesser pulse variability compared to Hybrid CSVCO by 15.67%, since Hybrid reverse CSVCO has current sources and sinks in IG configuration. In Pignsg due to loss of back channel, lesser variation in pulse width is observed compared to SG CSVCO. Psgnig CSVCO shows comparable variability to IG CSVCO. The variability in pulse width with t_{si} for MIGFET CSVCO is reduced by 18.6% compared to SG CSVCO.

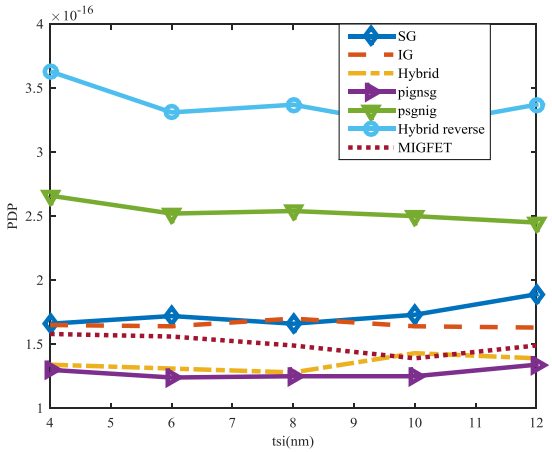


Figure 4.52: Variation of PDP of DG FinFET CSVCO variants with t_{si} for sub threshold operation

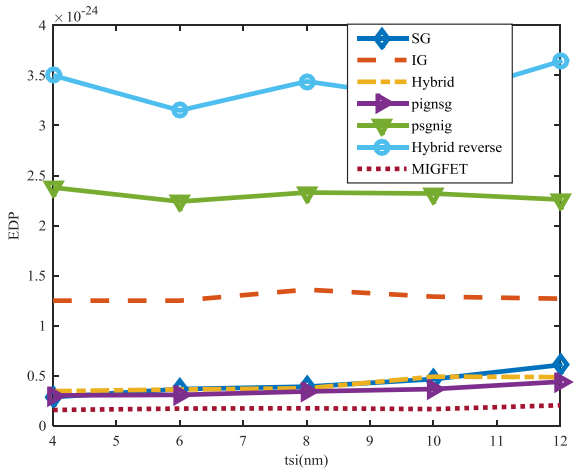


Figure 4.53: EDP variation sensitivity of DG FinFET CSVCO variants with t_{si} for sub threshold operation

Pignsg exhibits least and almost constant PDP as shown in Figure 4.52 whereas EDP for MIGFET CSVCO is least and remains almost constant with increase in t_{si} as shown in Figure 4.53.

Figure 4.54, 4.55 and 4.56 shows the variation of pulse width, PDP and EDP respectively for all CSVCO configurations with supply voltage variation.

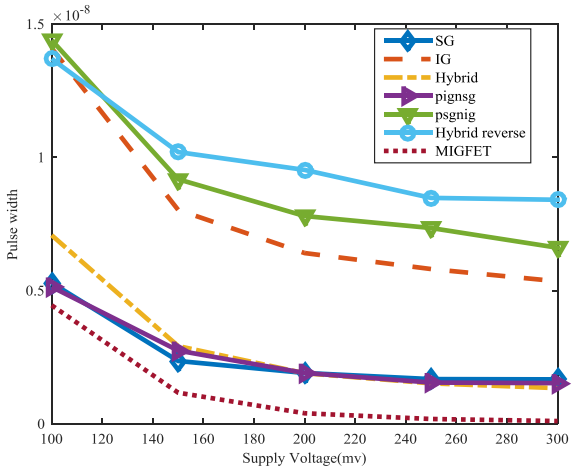


Figure 4.54: Variation of pulse width of DG FinFET CSVCO variants with supply voltage for sub threshold operation

The pulse width varies by 97.6% with variation in supply voltage from 100mV to 300mV for MIGFET CSVCO. SG CSVCO exhibit less pulse width variability with supply voltage variation compared to MIGFET CSVCO by 29.2%. In IG CSVCO, the pulse width variability with variation in supply voltage is reduced by 6.4% compared to SG CSVCO. Hybrid CSVCO shows increase in pulse width variability, with supply voltage variations, compared to SG CSVCO by 12.67%. As the transconductance of Pignsg CSVCO is lesser than Hybrid CSVCO, Pignsg CSVCO exhibits lesser pulse variability compared to Hybrid CSVCO by10.84%. It is observed that Psgnig exhibit lesser pulse width variability compared to SG CSVCO by 14.31%. Thus, with supply voltage variation Hybrid and MIGFET CSVCO shows increase in pulse width variation by 10.84% and 27% respectively compared to pignsg CSVCO as depicted in Figure 4.54.

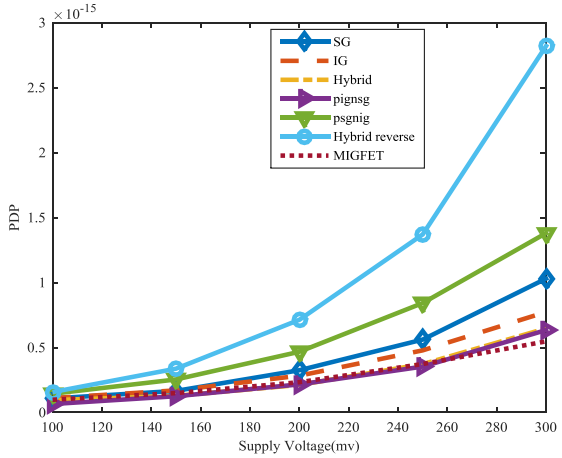


Figure 4.55: Variation of PDP of DG FinFET CSVCO variants with supply voltage for sub threshold operation

PDP increases with supply voltage and its variation is nearly same for pignsg and

MIGFET CSVCO as shown in Figure 4.55. EDP variation in MIGFET CSVCO is increased by 21% compared to pignsg CSVCO.

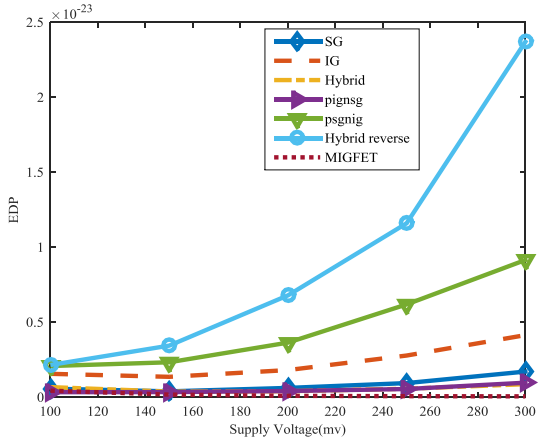


Figure 4.56: EDP variation sensitivity of DG FinFET CSVCO variants with supply voltage variation for sub threshold operation

Figure 4.57, 4.58 and 4.59 shows the variation in pulse width, PDP and EDP respectively for all CSVCO configurations with variation in temperature.

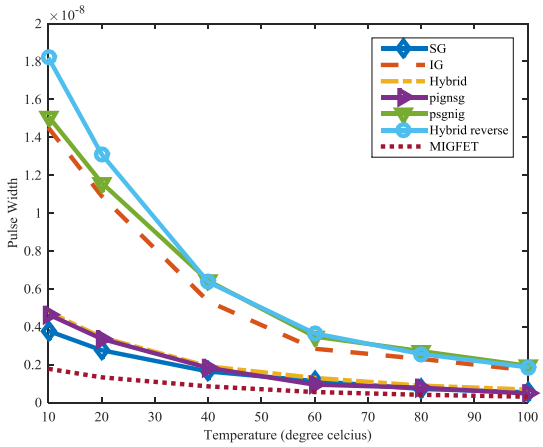


Figure 4.57: Variation of pulse width of DG FinFET CSVCO variants with temperature for sub threshold operation

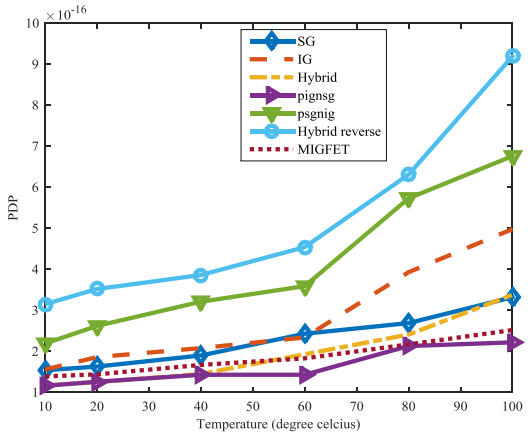


Figure 4.58: Variation of PDP of DG FinFET CSVCO variants with temperature for sub threshold operation

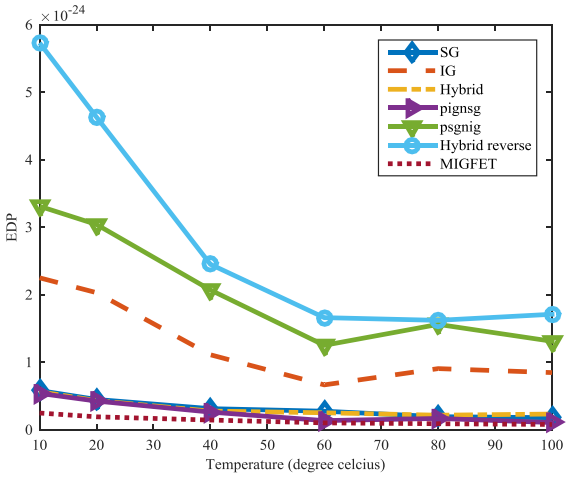


Figure 4.59: EDP variation sensitivity of DG FinFET CSVCO variants with temperature variation for sub threshold operation

The pulse width variability in pignsg is increased by 7% compared to MIGFET CSVCO as indicated by Figure 4.57.

PDP is least for pignsg CSVCO and its variation for pignsg CSVCO and MIGFET CSVCO is comparable as shown in Figure 4.58. EDP variation is increased by 11% in pignsg CSVCO compared to MIGFET CSVCO as shown in Figure 4.59.

Table 4.3 summarizes the frequency and power consumption of various DG FinFET CSVCO variants and Table 4.4 summarizes the variability results. From the results it can be concluded that even though MIGFET CSVCO exhibits better output frequency, it is very sensitive to supply voltage variations.

Table 4.3: Summary of performance and power consumption of DG FinFET CSVCO configurations

CSVCO Configuration	Frequency (MHz)	Power (nW)	Frequency –Power ratio (MHz/nW)
SG	212	70.3	3.015647
IG	62.2	21.2	2.93396
Hybrid	171	43.9	3.895216
Hybrid reverse	49	33	1.484848
pignsg	182	45.4	4.008811
psgnig	54.5	27.6	1.974638
MIGFET	426	127	3.354331

Table 4.4: Summary of variability results of DG FinFET CSVCO configurations

CSVCO Configuration	Oxide thickness variation			tsi variation			Supply voltage variation		
	%variation in pulse width	%variation in PDP	%variation in EDP	%variation in Pulse width	%variation in PDP	%variation in EDP	%variation in Pulse width	%variation in PDP	%variation in EDP
SG	48.60	3.5	50.42	46	10.2	52.79	68.4	89.5	66.60
IG	35.18	7.32	30.25	3.32	1.21	1.57	62	85.6	62.3
Hybrid	34.50	11.72	25.6	26.5	3.50	28.9	81.07	85.3	22.55
Hybrid	32.01	17.36	17.57	10.83	7.16	3.84	38.61	94.4	90.9
Pignsg	36.50	10.3	29.05	28.8	3	31.13	70.23	89.7	65.39
Psgnig	28.2	16.84	13.8	2.82	7.89	5.04	54.09	89.56	77.3
MIGFET	28.3	10.6	19.9	27.7	5.69	22.92	97.6	82	86.72

Pignsg CSVCO shows better results in terms of frequency obtained versus power expended giving least PDP of 1.25E-16, compared to all the CSVCO configurations. Also pulse width variability with supply voltage variation, is reduced by 27% in pignsg CSVCO compared to MIGFET CSVCO. Moreover, pignsg CSVCO shows almost same pulse variability to t_{si} variation, as that of MIGFET CSVCO. The pulse variability of pignsg CSVCO is increased by 8% and 7% for oxide thickness and temperature variation respectively as compared to MIGFET CSVCO. Therefore, taking the overall results into considerations, pignsg CSVCO can be considered as an optimal choice for sub threshold applications. A comparison of proposed VCO with existing VCO in literature is presented in Table 4.5

Table 4.5: Summary of proposed VCO with existing VCO in literature

	126	**46**	**41**	**58**	**67**	**68**	**This work**
Technology (nm)	130 CMOS	130 CMOS	130 CMOS	90 CMOS	50 DGMOS	15 FinFET	32 FinFET
Frequency (MHz)	5.65	1.52	4	5.12	6590	1800	182
Power (nW)	720	320	3.6	24	-	430	45.4
Frequency-Power ratio (MHz/nW)	0.007	0.004	1.1	0.2	-	4.18	4

4.6 Performance Analysis of CNFET based Clock Generator Circuits

This section investigates the viability of CNFET based CSVCO in sub threshold regime. Performance comparison of CMOS and CNFET based CSVCO is reported in this section. Four CNFET based CSVCO configurations viz. CNFETVCO-1, CNFETVCO-2, CNFETVCO-3 and CNFETVCO-4 are designed at 32 nm technology node using Stanford CNFET model and are simulated using HSPICE to investigate the optimal configuration for sub threshold applications. CNFETVCO-3 is optimized to improve the performance. Furthermore, Optimized CNFETVCO-3 performance is compared to CMOS based VCO and DG FinFET based pignsg VCO.

4.6.1 Performance Comparison of Bulk CMOS and CNFET Based VCO

This sub-section investigates the performance of bulk CMOS based CSVCO and CNFET based CSVCO in sub threshold region. A five stage CMOS based CSVCO, as shown in Figure 3.6 in chapter 3, is designed at 32 nm technology node using PTM [90] and CNFET based CSVCO circuit, as shown in Figure 3.21 is designed at 32nm technology node with Stanford CNFET model [116].

In order to investigate the tuning range, CMOS based and CNFET based CSVCO circuit are simulated by varying the control voltage at 125mV supply voltage. The results are depicted in Figure 4.60. The variation in control voltage from 50mV to 125mV gives the variation in frequency from 175 KHz to 439 KHz and 30.6 MHz to 129 MHz for CMOS and CNFET VCO respectively.

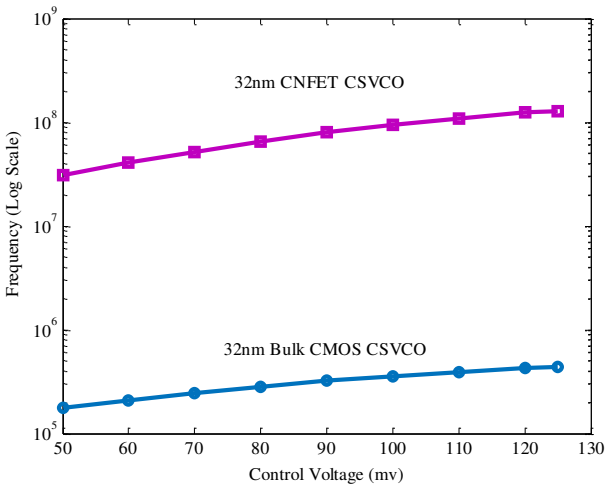
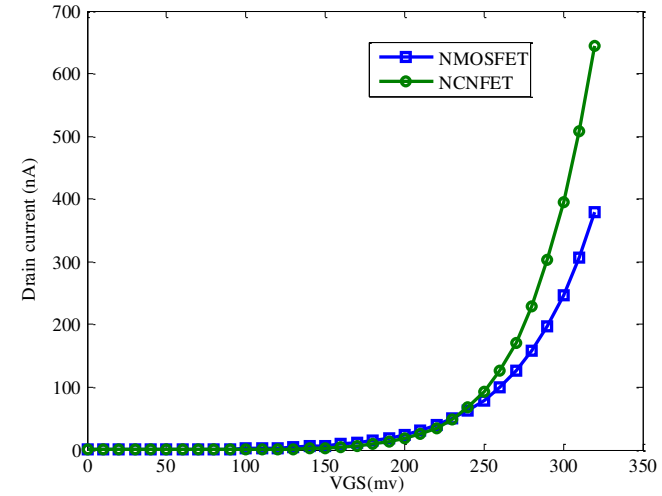


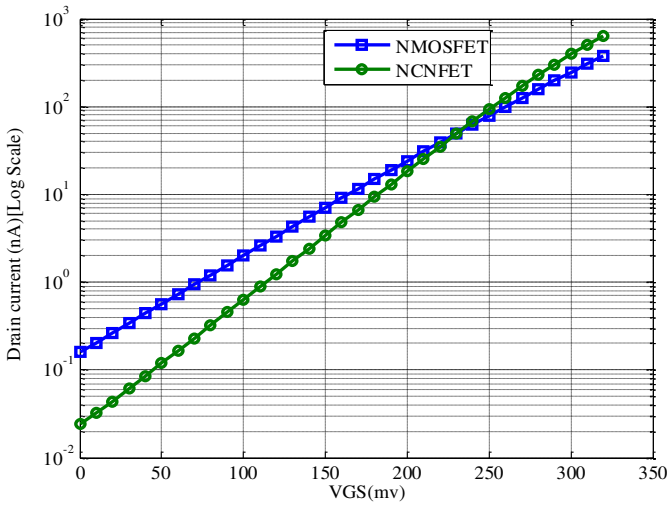
Figure 4.60: Tuning characteristics of CMOS and CNFET based VCO

The ballistic transport improves the performance of CNFET VCO. To observe the sub threshold slope of CNFET and MOSFET, a 32nm N type MOSFET with 64 nm

width and 32nm NCNFET with (n,m) = (17,0) and number of nanotubes for CNFET=2, back gate=0V are simulated by varying V_{GS} and corresponding V-I characteristics is depicted in Figure 4.61 (a) and 4.61 (b). The results indicate that the sub threshold slope and performance of CNFET is improved compared to MOSFET. CNFET and MOSFET shows sub threshold slope of 70mV/decade and 90mV/decade respectively. The improved sub threshold slope supplemented with ballistic transport improves the performance of CNFET VCO.



(a)



(b)

Figure 4.61: Drain current variation for change in gate to source voltage for 32nm N type MOSFET and 32nm NCNFET (a)-Linear scale (b)Log scale

Figure 4.62 shows the power variation with variation in control voltage for CMOS and CNFET based VCO. CNFET shows increase in power consumption compared to CMOS VCO

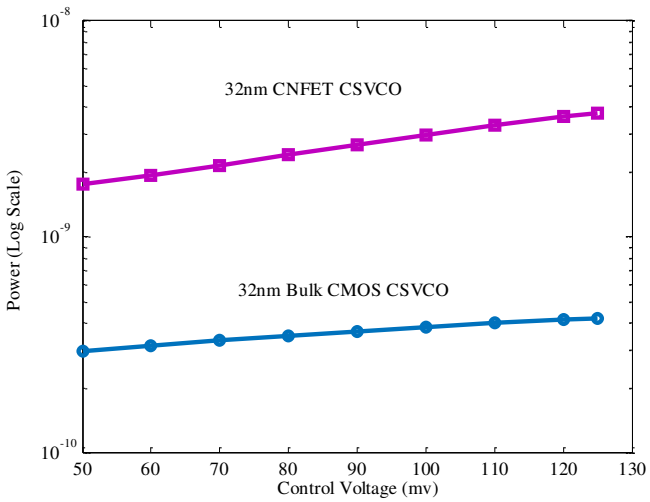


Figure 4.62 Variation in power with variation in control voltage

. PDP of Bulk CMOS CSVCO and CNFET CSVCO are investigated and its variation with supply voltage is depicted in Figure 4.63. Though CNFET shows increase in power consumption compared to CMOS VCO, the PDP of CNFET CSVCO is improved by about 97% compared to Bulk CMOS CSVCO at supply voltage of 125mV at room temperature as shown in Figure 4.63. PDP increases exponentially with increase in supply voltage for both CMOS based VCO as well as CNFET based VCO.

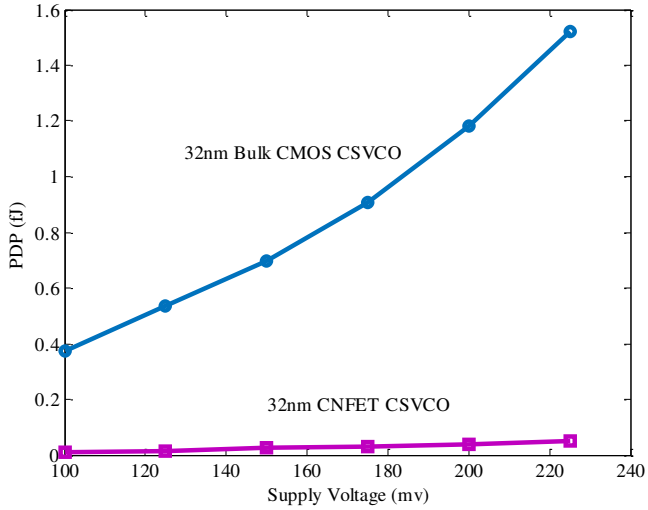


Figure 4.63: PDP comparison of Bulk CMOS and CNFET CSVCO with variation in supply voltage

EDP of Bulk CMOS and CNFET based CSVCO is explored and plotted in Figure 4.64. EDP of CNFET CSVCO is lesser by 8833 times compared to Bulk CMOS CSVCO at supply voltage of 125mV.

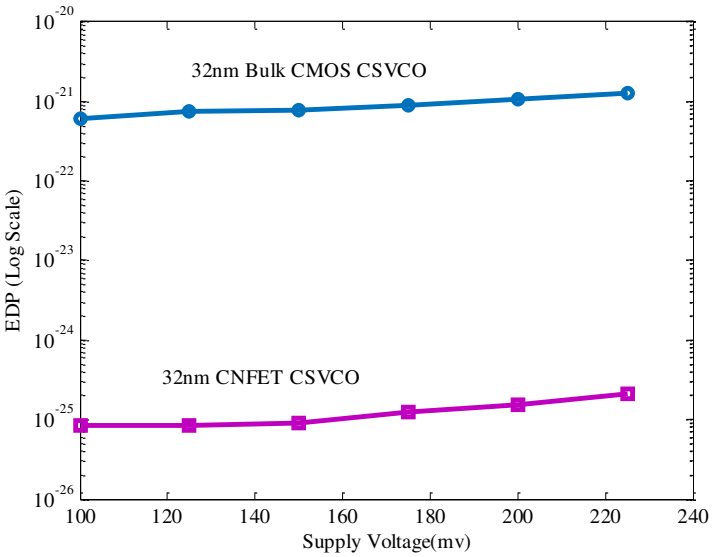


Figure 4.64: EDP comparison of Bulk CMOS and CNFET CSVCO with variation in supply voltage.

Monte Carlo simulations are performed in order to investigate the impact of overall PVT variations on CSVCO output pulse width and EDP. ±10% variation in V_{th}, ±10% variation in supply voltage and ±20% variation in temperature is considered for bulk CMOS VCO and ±10 % variation in diameter, ±10% variation in supply voltage and ±20% variation in temperature is considered for CNFET VCO.

Figure 4.65 and 4.66 shows the variation ion pulse width for bulk CMOS and CNFET VCO respectively. The spread in pulse width is reduced in CNFET CSVCO compared to bulk CMOS CSVCO exhibiting the improved robustness in CNFET.

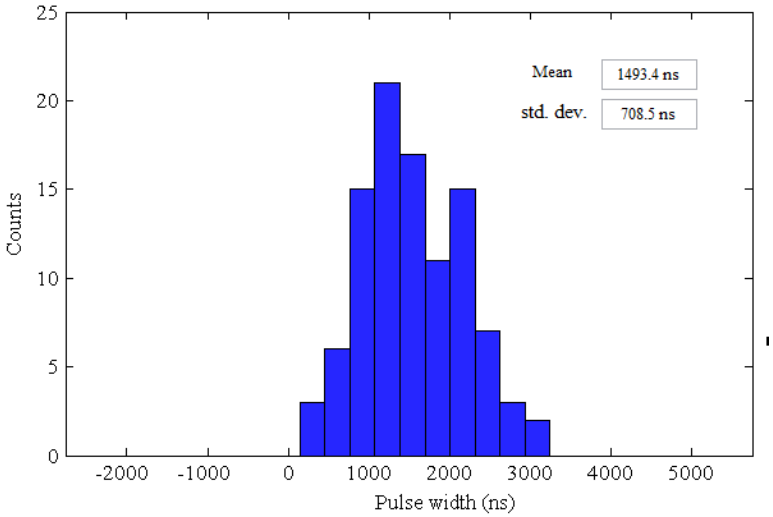


Figure 4.65: PDF for bulk CMOS CSVCO

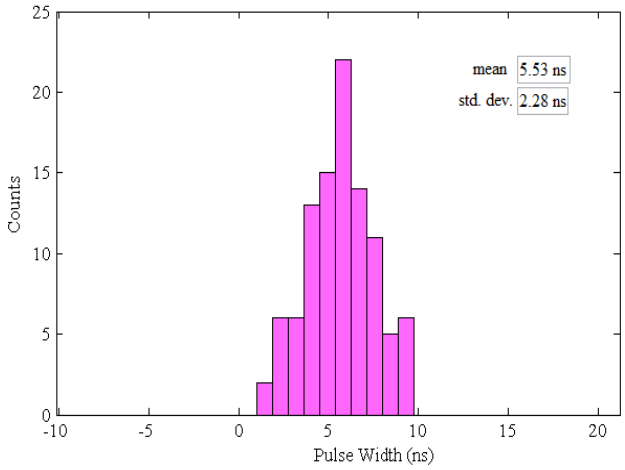


Figure 4.66: PDF for CNFET CSVCO

Figure 4.67 and 4.68 illustrates the spread in EDP in bulk CMOS CSVCO and CNFET CSVCO respectively. The spread in EDP is reduced in CNFET based CSVCO compared to bulk CMOS by almost 22%.

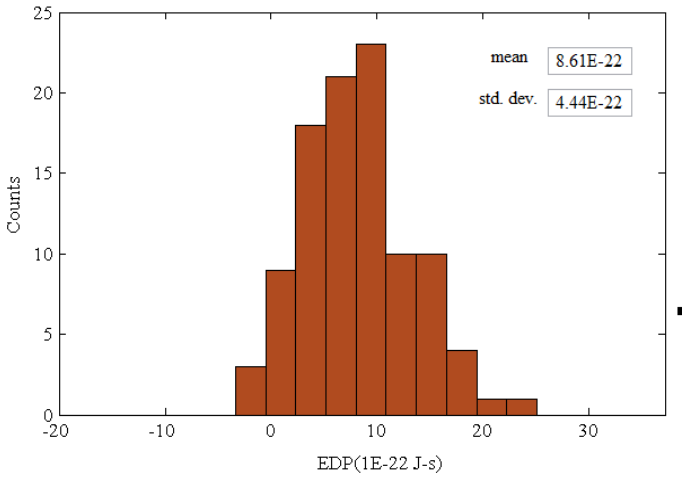


Figure 4.67: PDF for bulk CMOS CSVCO

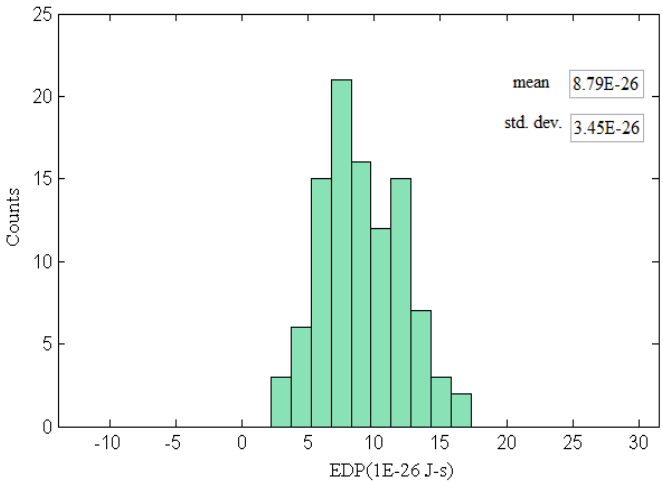


Figure 4.68: PDF for CNFET CSVCO

4.6.2 Performance Analysis of Various Configurations of CNFET Based VCO

Four CNFET based CSVCO configurations are designed as discussed in section 3.7.1 of chapter 3 and are simulated in HSPICE at supply voltage V_{DD} of 100mV and control voltage, $V_{control}$ of 100mV at 25°C temperature. The simulation results are enumerated in Table 4.6.

Table 4.6: Comparison of performance parameters of various CNFET CSVCO configurations

CSVCO Configurations				
	CNFETVCO-1	**CNFETVCO-2**	**CNFETVCO-3**	**CNFETVCO-4**
Pulse width(ns)	7.39	11.2	6.05	14.4
Frequency(MHz)	67.9	44.5	82.7	34.7
Power(nW)	0.34	0.481	0.454	0.365
PDP (J)	2.50E-18	5.40E-18	2.74E-18	5.26E-18
EDP(J-s)	1.84E-26	6.07E-26	1.66E-26	7.58E-26

As indicated in Table 4.6, CNFETVCO-3 exhibits better output frequency compared to other configurations. The enhanced drive current supplemented with reduced gate capacitance proliferate the performance of CNFETVCO-3. The pulse width in CNFETVCO-3 is reduced by 18.13% and EDP is improved by 9.78% at the cost of increase in PDP by 8.7% as compared to CNFETVCO-1 whereas the pulse width in CNFETVCO-3 is reduced by 45.98% and EDP is improved by 72.65% compared to CNFETVCO-2. CNFETVCO-4 shows increase in pulse width by 48.68% compared to CNFETVCO-1 and 57.98% compared to CNFETVCO-3. EDP of CNFETVCO-4 is increased by 75.72% compared to CNFETVCO-1 and 78.1% compared to CNFETVCO-3. Thus as can be inferred from Table 4.6, CNFETVCO-3 exhibits better performance compared to all other configurations.

In order to observe the impact of supply voltage on pulse width, PDP and EDP of VCO, the supply voltage, V_{DD} is varied from 80mV to 225mV with constant control voltage, $V_{control}$ of 100mV. Figure 4.69-4.71 respectively illustrates the variation in pulse width, PDP and EDP for all the four configurations with variation in supply voltage.

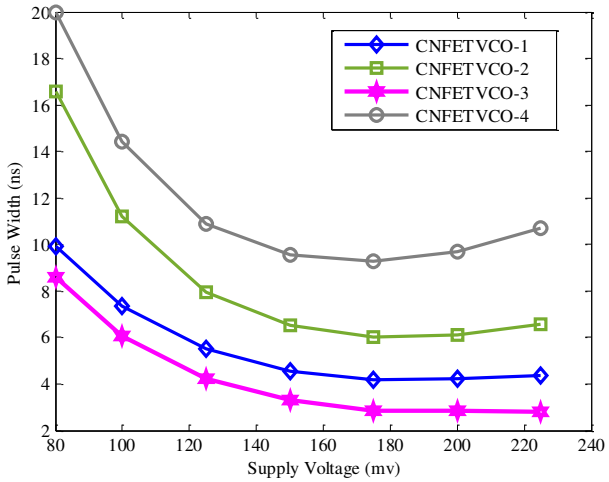


Figure 4.69: Variation of Pulse Width of CNFETVCO variants with supply voltage for sub threshold operation

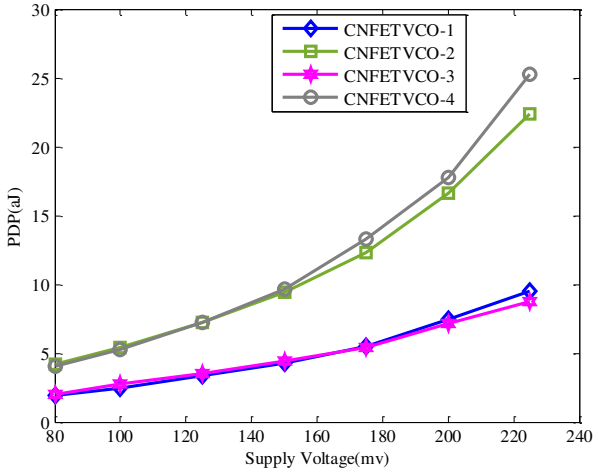


Figure 4.70: Variation of PDP of CNFETVCO variants with supply voltage for sub threshold operation

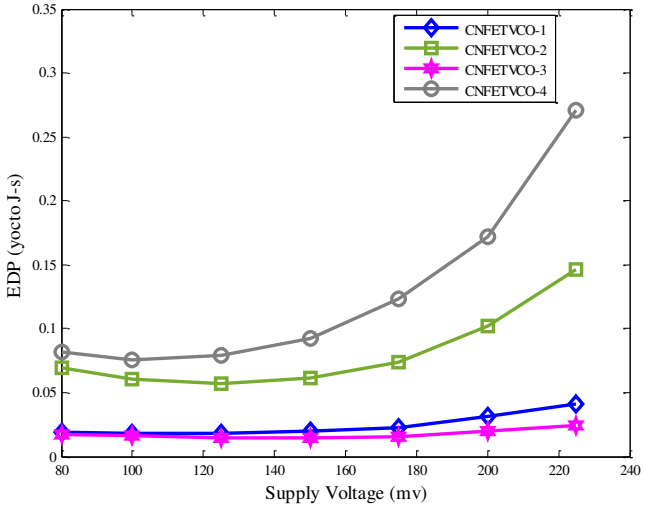


Figure 4.71: EDP variation of CNFETVCO variants with supply voltage variation for sub threshold operation

As supply voltage is reduced from 225mV to 80mV, pulse width increases whereas PDP and EDP decrease exponentially

Simulations are performed by varying the control voltage in order to explore the tuning range of CNFETVCO variants at supply voltage of 100mV. Control voltage is varied from 50mV to 100mV and the corresponding variation in frequency for CNFETVCO variants is depicted in Figure 4.72.

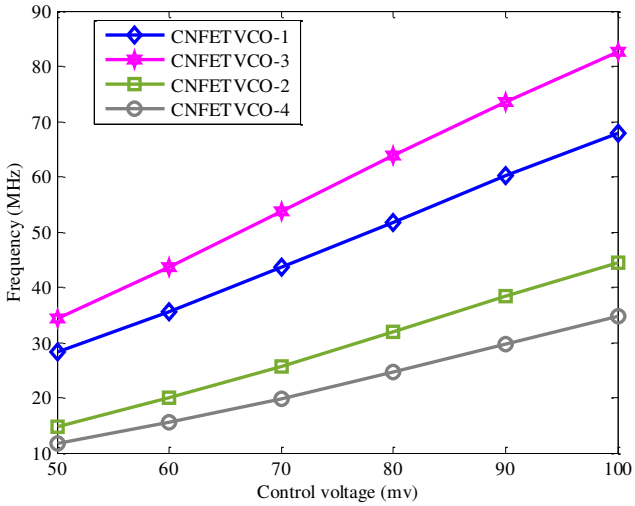


Figure 4.72: Frequency variation with control voltage variation

All CNFETVCOs exhibits linear tuning characteristics. CNFETVCO-3 shows the widest tuning range with frequency varying from 34.3 MHz to 82.7 MHz.. The variation in power with control voltage variation is depicted in Figure 4.73.

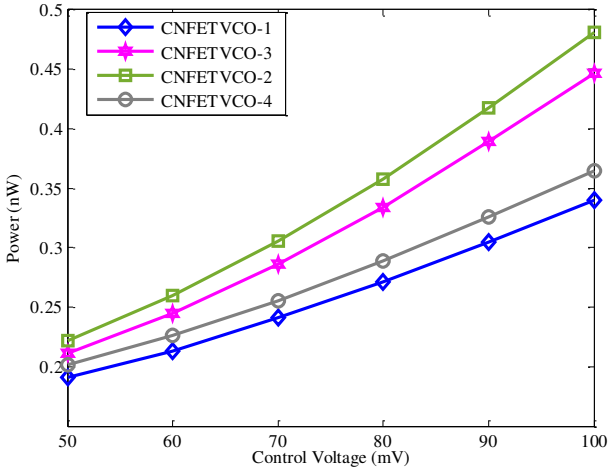


Figure 4.73: Power variation with control voltage variation

Table 4.7 indicates the performance parameters of CNFETVCO variants with variation in control voltage.

Table 4.7: Performance parameters of various CNFET CSVCO configurations with varying control voltage

CNFETVCO Variant	Frequency (MHz)		Power (nW)	
	Min	**Max**	**Min**	**Max**
CNFETVCO-1	28.2	67.9	0.191	0.340
CNFETVCO-2	14.8	44.5	0.222	0.481
CNFETVCO-3	34.3	82.7	0.211	0.447
CNFETVCO-4	11.7	34.7	0.202	0.365

Figure 4.74 shows the impact of temperature variation on PDP of CNFETVCO configurations. Because of high thermal stability exhibited by CNTs in CNFET, PDP remains almost constant with variation in temperature from 10 °C to 100 °C.

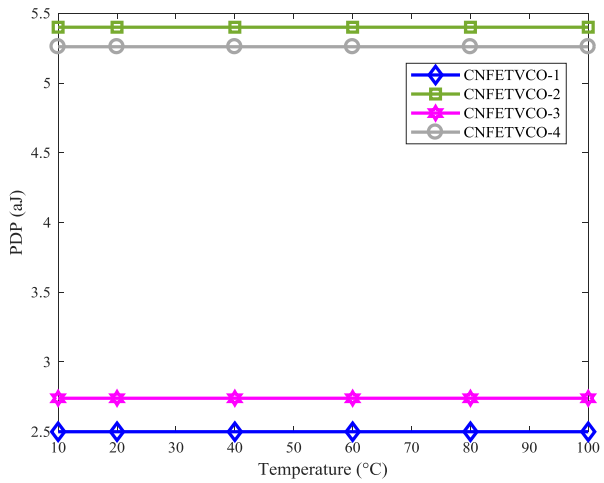


Figure 4.74: Variation of PDP of CNFETVCO variants with variation in temperature for sub threshold operation

To observe the impact of variation in diameter on pulse width, positive integers m and n, that specify the chirality vector are varied and the impact of its variation on pulse width is depicted in Figure 4.75. Increase in diameter offers higher current drive which is reflected in decrease in pulse width as shown in Figure 4.75. CNFETVCO-4 exhibits highest sensitivity to diameter variations whereas CNFETVCO-3 exhibits lowest pulse variability compared to other CNFETVCO configuration, as can be seen from Figure 4.75. CNFETVCO-4 exhibits more pulse variability compared to all other configurations.

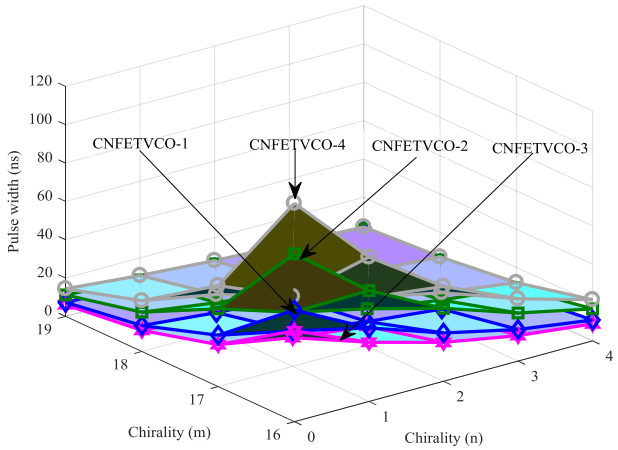


Figure 4.75: Variation of pulse width of CNFETVCO variants with variation in chirality vector

PDP remains constant with change in chirality vector and thereby diameter as shown in Figure 4.76. Energy delay product (EDP) is more biased to delay compare to power and hence exhibits the same trend as delay as shown in Figure 4.77

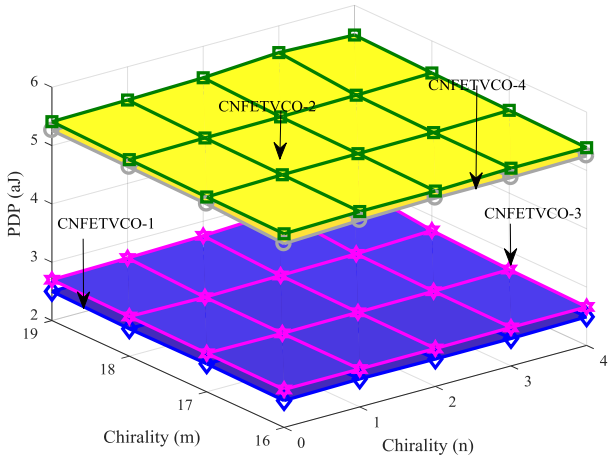


Figure 4.76: Variation of PDP of CNFETVCO variants with variation in chirality vector

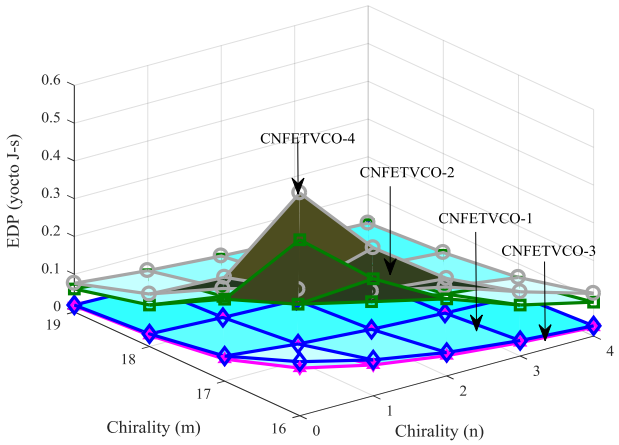


Figure 4.77: Variation of EDP of CNFETVCO variants with variation in chirality vector

Thus the results discussed in this section indicate that CNFETVCO-3 exhibits better performance as well as robustness compared to other configurations..

4.6.3 Optimization of CNFETVCO-3

This section deals with optimization of various structural device parameters of CNFET like number of nano tubes, pitch, diameter and oxide thickness.

- **Selection of optimum number of CNT's**

CNFETVCO-3 is simulated considering diameter of CNTs in all CNFETs= 1.5nm, pitch=20nm and number of tubes in CNFETs of inverter =3. The simulation results are depicted in Figure 4.78. Even-though the pulse width reduces with increase in number of nano tubes, PDP increases correspondingly as evident from Figure 4.78. As seen in Figure 4.78, the product of pulse width and PDP is minimum for number of tubes =9. Therefore for further analysis N=9 is considered for CNFETs in current source and sinks to have high performance energy efficient CNFETVCO-3.

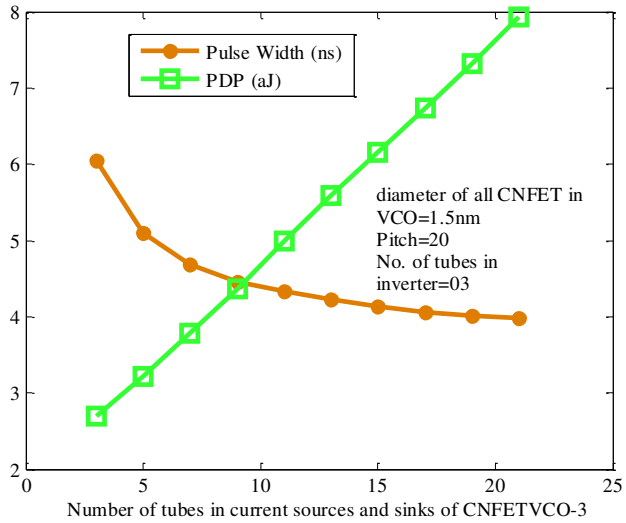


Figure 4.78: Pulse Width and PDP as a function of number of tubes of CNFETs in current sources and sinks

- **Selection of optimum pitch**

Considering diameter of CNTs in all CNFETs= 1.5nm, pitch=20nm for CNFETs in inverter, number of tubes in CNFETs of inverter =3 and number of tubes in CNFETs of current source and sinks =9, CNFETVCO-3 is simulated to investigate the optimal pitch for CNFETs in current sources and sinks.

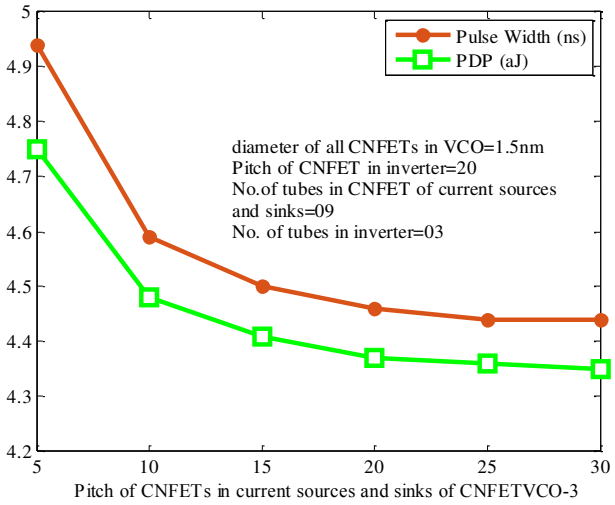


Figure 4.79: Pulse Width and PDP as a function of pitch for tubes in CNFETs of current sources and sinks

The simulation results are shown in Figure 4.79. As evident from Figure 4.79, pulse width as well as PDP reduces with increase in pitch and the pulse width almost becomes constant beyond 20nm pitch. Therefore optimum value of pitch, P is selected to be 20nm for further simulations.

- **Selection of optimum CNFET diameter**

To investigate the optimum value of CNT diameter for all CNFETs, the simulation of CNFETVCO-3 is carried out considering pitch =20nm, N=3 for CNFETs in inverters and N=9 for CNFETs in current source and sinks. The result is depicted in Figure 4.80. From Figure 4.80, diameter of tubes of all CNFETs is chosen to be equal to 1.5nm to have an energy efficient CNFETVCO-3 with better performance.

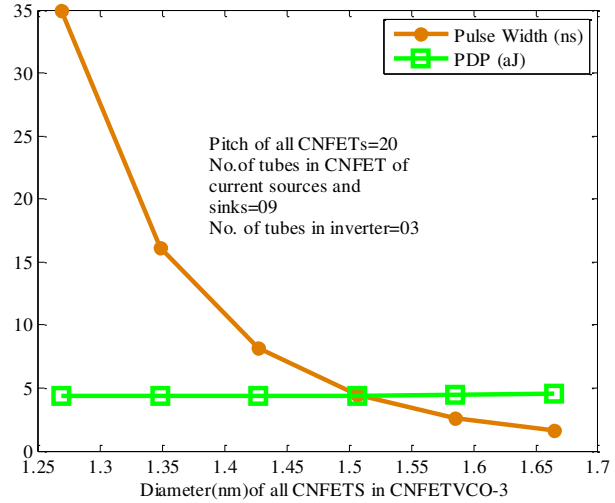


Figure 4.80: Pulse Width and PDP as a function of diameter of tubes of all CNFETs

- **Selection of optimum oxide thickness**

To investigate optimal oxide thickness, CNFETVCO-3 is simulated considering pitch=20nm, diameter=1.5nm, N=3 for CNFETs in inverters and N=9 for CNFETs in current source and sinks. The simulation results are depicted in Figure 4.81. As can be inferred from Figure 4.81, pulse width and PDP reduces with reduction in oxide thickness. The oxide thickness chosen is 1.5nm for further simulation.

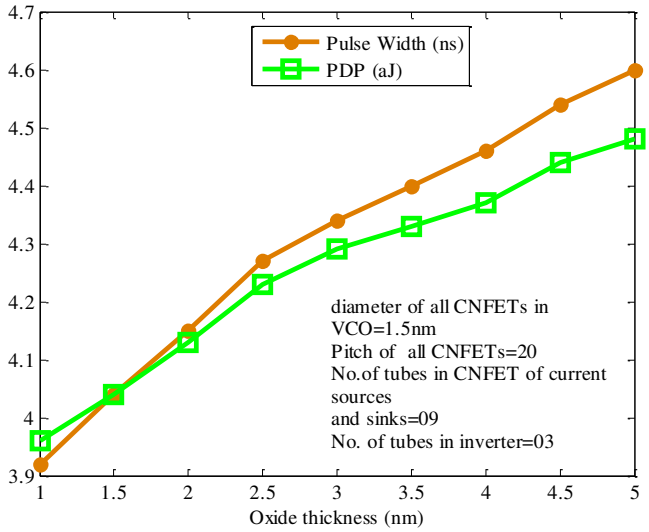


Figure 4.81: Pulse Width and PDP as a function of oxide thickness

4.6.4 Evaluation of Optimized CNFETVCO-3

Figure 4.82 depicts the performance parameters of CNFETVCO variants.

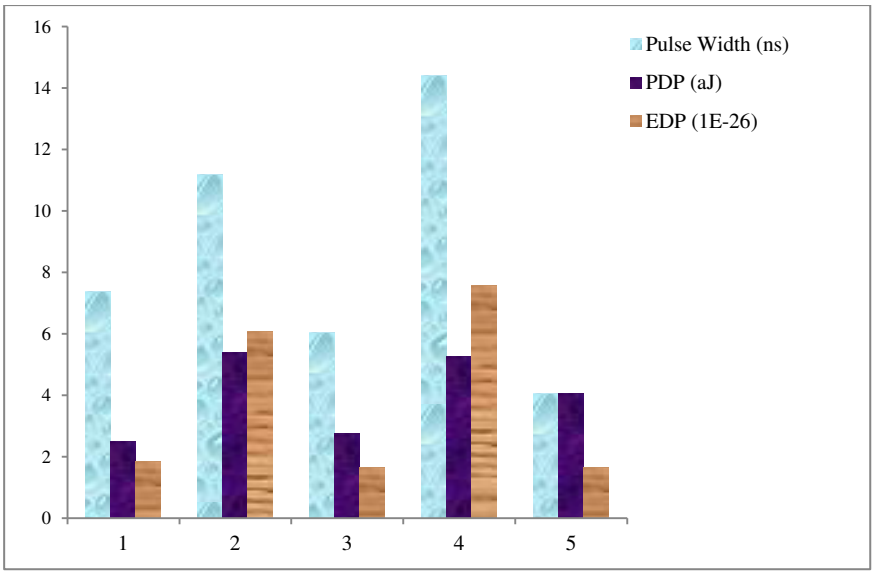


Figure 4.82: Performance comparisons of various CNFETVCO configurations

1-CNFETVCO-1, 2-CNFETVCO-2, 3-CNFETVCO-3, 4-CNFETVCO-4, 5-Optimized CNFETVCO-3

Optimized CNFETVCO-3 shows improved performance as indicated by Figure 4.82. The output pulse width is reduced in optimized CNFETVCO by 33.2% compared to CNFETVCO-3. However this improvement in performance of optimized CNFETVCO-3 comes at the cost of increase in PDP by 32.17% compared to CNFETVCO-3 exhibiting power-performance trade off.

CNFETVCO-3 and optimized CNFETVCO-3 shows comparable EDP. Figure 4.83 demonstrates the improved tuning performance of optimized CNFETVCO-3 over CNFETVCO-3. Variation in power for optimized CNFETVCO-3 and CNFETVCO-3 is shown in Figure 4.84.

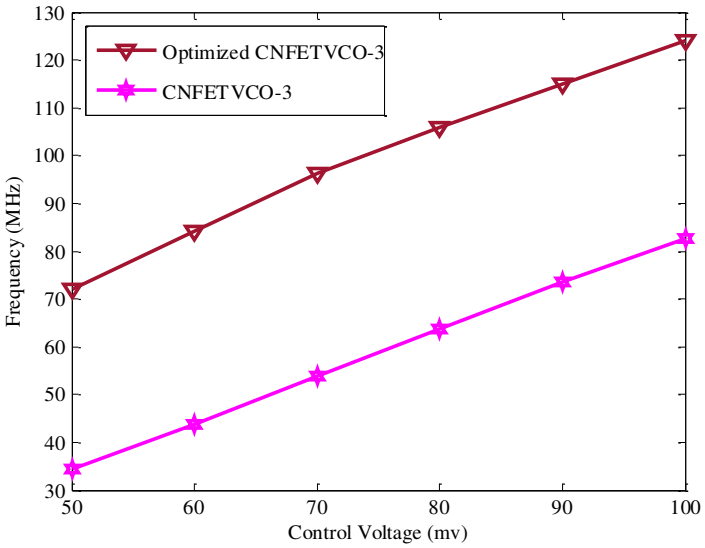


Figure 4.83: Tuning characteristics of CNFETVCO -3 and optimized CNFETVCO-3

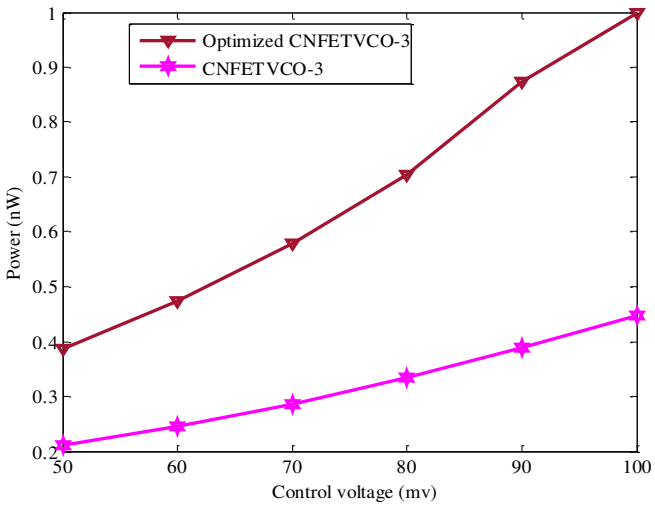


Figure 4.84: Variation in power with variation in control voltage

To investigate the overall impact of PVT variation on CNFETVCO output, Monte Carlo simulations are performed considering ±10% variation in diameter, ±10% variation in supply voltage and ±10% variation in temperature and results are depicted in Figure 4.85.

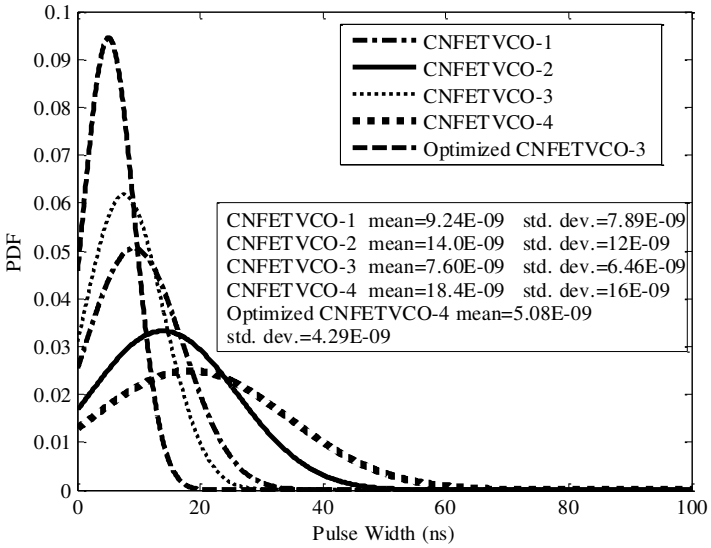


Figure 4.85: PDF for CNFETVCO variants

The simulation results reveal that optimized CNFETVCO-3 exhibit better robustness compared to other configurations.

Thus it can be concluded that optimization of CNFETVCO-3 brings about improvement in speed and robustness. A comparison of proposed VCO with existing state-of-the-art VCOs is presented in Table 4.8

Table 4.8: Summary of proposed VCO with existing VCO in literature

Reference	**[40]**	**[57]**	**[67]**	**[123]**	**[124]**	***This work***
Technology (nm)	130 CMOS	90 CMOS	15 FinFET	32 FinFET	32 CNFET	32 CNFET
Frequency (MHz)	4	5.12	1800	182	150000	82.7
Power(nW)	3.6	24	430	45.4	40000	0.447
Frequency-Power ratio(MHz/nW)	1.1	0.2	4.18	4	3.75	185

The results in Table 4.8 indicate that the Optimized CNFETVCO-3 exhibits better performance in terms of frequency obtained versus power expended.

4.7 Performance Comparison of CMOS, Pignsg DG Fin FET and Optimized CNFETVCO-3 circuit.

CMOS VCO, DG FinFET pignsg VCO and optimized CNFETVCO-3 VCO are simulated in HSPICE at supply voltage of 150mV. The simulation results are depicted in Figure 4.86 and 4.87.

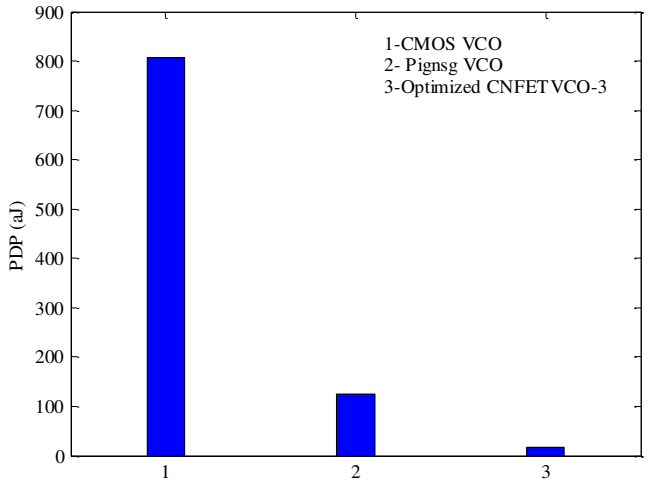


Figure 4.86: PDP comparison of CMOS, DG FINFET pignsg and Optimized CNFETVCO-3

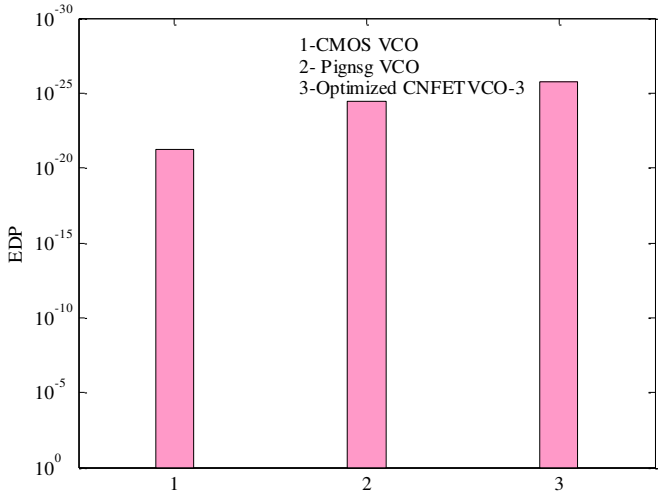


Figure 4.87: EDP comparison of CMOS , DG FINFET pignsg and Optimized CNFETVCO-3

Delay in Optimized CNFETVCO-3 is reduced by 99.87% and 67.27% as compared to CMOS VCO and DG Fin-FET pignsg VCO respectively. PDP is improved by 97.75% and 85.52% in Optimized CNFETVCO-3 compared to CMOS VCO and DG

Fin-FET pignsg VCO respectively whereas EDP is improved by 99.99% and 95.21% in Optimized CNFETVCO-3 compared to CMOS VCO and DG Fin-FET pignsg respectively. Thus, the results indicate that the CNFET based optimized CNFETVCO-3 exhibits better performance in terms of speed as well energy efficiency.

Monte Carlo simulations were performed in order to investigate the robustness of CMOS VCO, DG Fin-FET, pignsg VCO and optimized CNFETVCO-3 by considering ±10% variation in threshold voltage and supply voltage and ±20% variation in temperature. The variation in pulse width with PVT variation in CMOS VCO, DG Fin-FET, pignsg VCO and optimized CNFETVCO-3 is depicted in Figure 4.88, 4.89and 4.90 respectively.

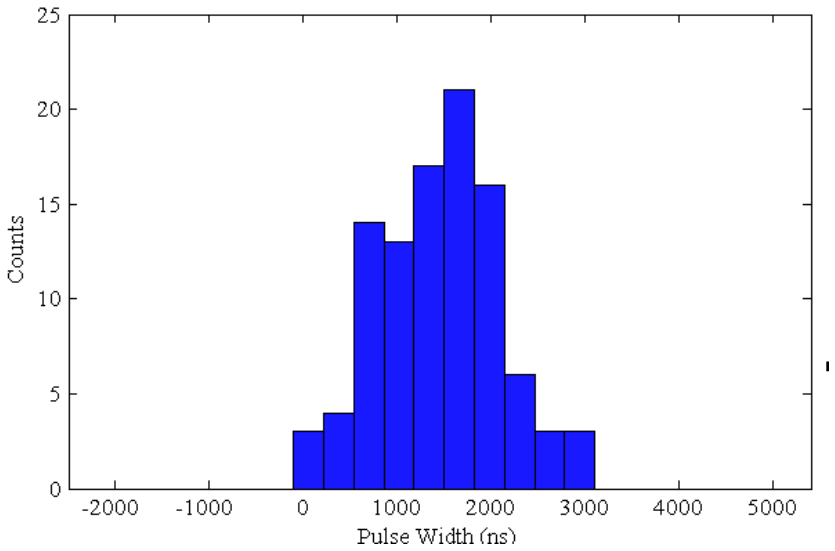


Figure 4.88: PDF for CMOS CSVCO

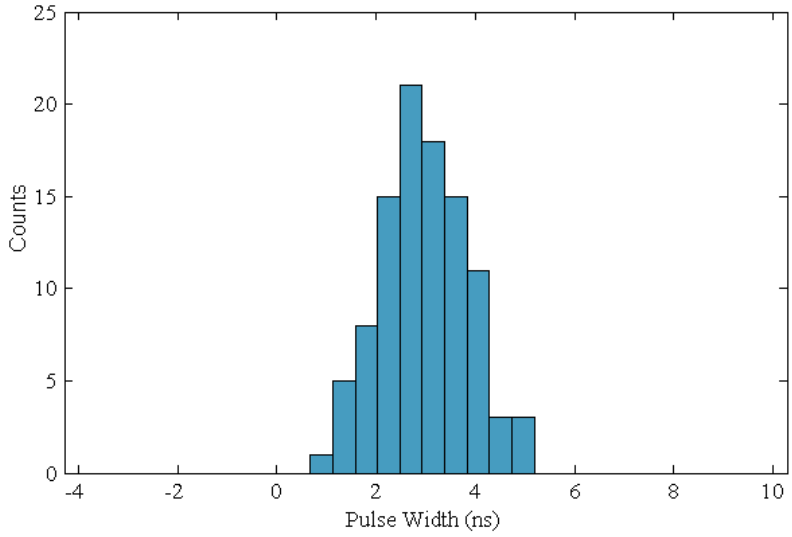


Figure 4.89: PDF for DG FinFET pignsg VCO

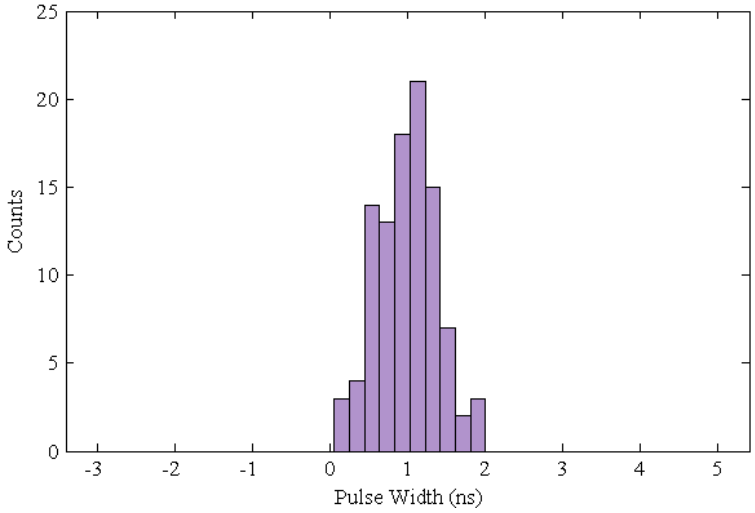


Figure 4.90: PDF for Optimized CNFETVCO-3

Figure 4.91, 4.92 and 4.93 depicts the variation in PDP for PVT variation in CMOS VCO, DG Fin-FET, pignsg VCO and optimized CNFETVCO-3 respectively.

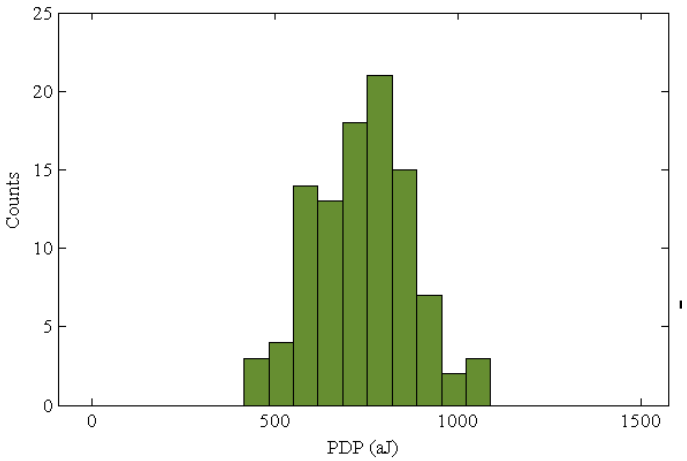


Figure 4.91: PDF for CMOS CSVCO

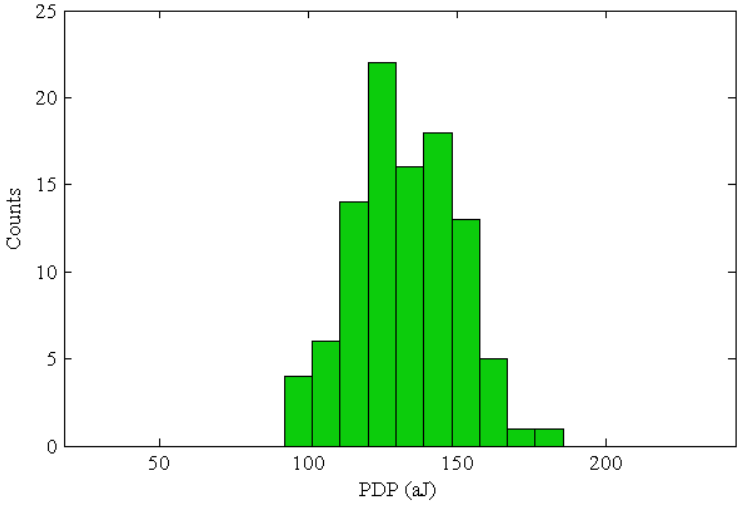


Figure 4.92: PDF for DG FinFET pignsg VCO

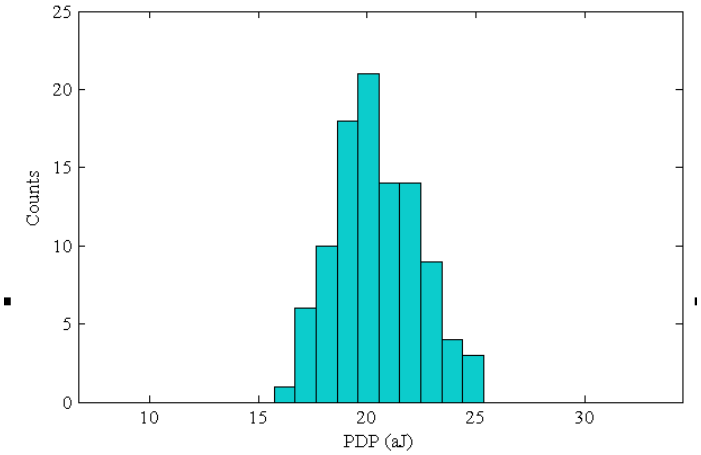


Figure 4.93: PDF for Optimized CNFETVCO-3

The spread in pulse width for optimized CNFETVCO-3 is reduced compared to other two VCOs. Thus, CNFETVCO-3 proves to be energy efficient and robust clock generator circuit and therefore can be proposed as an optimal clock generator in sub threshold regime.

4.8 Summary

This chapter explored the impact of supply voltage scaling on clock system parameters. It further explored the suitability of buffered and un-buffered clock system in sub threshold regime. It investigated the suitability of conventional CDN for sub threshold regime and proposed an optimized uniform H tree with CMOS buffer connected to clocked element followed by DTMOS buffer. Furthermore, this chapter discussed the simulation results obtained by simulating various schematics of clock circuits with CMOS and devices beyond CMOS. A comparative analysis of CMOS based, Fin-FET based and CNFET based VCO revealed that CNFET based CNFETVCO-3 is an optimal choice for sub threshold clock circuit.

Chapter 5

CONCLUSIONS AND FUTURE SCOPE

The unprecedented success of semiconductor industry has led to the development of CMOS integrated circuits at a very fast pace. The electronic systems are shrinking and system on chip is becoming vital for the emerging portable applications. But this has increased the power density and hence power has emerged as an important design metric. Sub threshold operation quenches the ULP demand of multitude of applications such as pace maker, RFID tags, biomedical sensors and wireless sensors. Low power consumption is an essential requirement for such applications since battery charging or replacement is infeasible. Clock circuit is a vital building block for such applications. Therefore, design of ULP clock circuit has great potential to have prolonged battery life. This work investigated the challenges in design of ULP clock circuit and explored the various techniques to enhance the performance and improve the robustness of ULP clock circuit

5.1 Conclusions

Clock circuit is a crucial and inevitable block in synchronous systems. Extensive research work has been carried out by the researchers to investigate the issues of clock circuit design in super threshold regime. From the review, it is clear that though researchers have provided the solutions to mitigate the issues of clock circuit design for high speed applications, the design of sub threshold clock circuit has not been explored much. Therefore, there is a need to investigate the design issues for ULP clock circuit and devise the techniques to cope up with these issues. Furthermore, the review highlights that although significant work has been carried out by the research community to combat the impact of temperature variation in the super threshold region, very few researchers have explored this area in the sub-threshold regime. Also as reported by ITRS, further scaling of bulk MOS technology is very difficult due to increased static power and variability issues. Therefore, there is need to investigate the viability of devices beyond CMOS for sub threshold clock circuit. This has provided the motivation to work in this area and to design ULP robust clock circuit.

Design of various schematics of clock circuit is presented in this work. CMOS based clock circuit is designed and clock circuit parameters are explored. The impact of process and PVT variation on the performance parameters of buffered and un-buffered clock system is observed. The observation reveals that the design of variability-resilient clock generator circuits for ULP applications at lower supply voltages is challenging because of reduced drive current and exacerbated variability. Furthermore, the variability analysis explored in this work indicates that the clock generator itself is dominating source for pulse width variation. Therefore techniques need to be devised to design stable VCO in sub threshold regime. The impact of temperature variation on clock generator in sub threshold and super threshold regime is investigated. It is observed that the exponential dependency of the time period on temperature in sub threshold regime is a major concern and hence calls for design of thermally aware ULP clock circuit. Thermal analysis of VCO is carried out and a scheme to improve the thermal stability of the sub threshold VCO is presented in this work. The simulation results of proposed thermally aware ULP clock generator system shows stable clock frequency over a wide range of temperature as compared to the conventional CSVCO circuit.

The performance comparison of buffered and un-buffered tree is reported in this work and the design of slew aware ULP CDN is discussed. By comprehensive analysis of results, it is concluded that clock system with un-buffered tree is a good option in sub threshold region. To improve the slew, the optimization of interconnect parameters along with conventional CMOS buffer connected to clocked elements followed by DTMOS buffer is proposed in his work. The results shows that the proposed CDN exhibits improved slew with additional benefit of reduced power consumption and improved robustness, compared to conventional CDN.

The performance analysis of DTMOS, CMOS and hybrid sub threshold clock generator circuits shows that DTCSVCO-2, a hybrid clock generator circuit exhibits better performance. Design of various schematics of ULP clock generator circuit with devices beyond CMOS is accentuated in this work. Performance comparison of CMOS and DG FinFET based CSVCO is presented. PDP, EDP and robustness of DG FinFET based CSVCO is improved as compared to Bulk CMOS CSVCO. Seven different configurations of five stages CSVCO have been explored to investigate the optimal configuration for sub threshold applications. The results revealed that pignsg

CSVCO proves to be a better configuration in terms of frequency obtained versus power expended as well as robustness compared to other configurations. This work investigated the viability of CNFET based ULP VCO and explored the performance of various configurations of CNFET based CSVCO. The analysis indicates that CSVCO using CNFET is a viable option for ULP system in nano-scale era. Four different configurations of five stages CNFETVCO have been designed and simulated using HSPICE to investigate the optimal configuration for sub threshold applications. The results indicate that CNFETVCO-3 proves to be a better configuration in terms of performance and robustness. CNFETVCO-3 is further optimized to improve the performance. The performance evaluation of optimized CNFETVCO-3 shows that the speed of ULP CNFET circuit can be enhanced by optimization of various CNFET parameters like number of CNT, diameter of CNT, pitch and oxide thickness. The optimized CSVCO-3 exhibits superior speed and robustness against PVT variation compared to CNFETVCO-3. Finally, the performance comparison of CMOS VCO, DG Fin-FET based pignsg VCO and optimized CNFETVCO-3 is reported in this work. The results show that that CNFET based optimized CNFETVCO-3 exhibits better performance in terms of energy efficiency as well as robustness.

5.2 Future Scope

The result of this work has touched to some aspects of the robust sub threshold clock circuit design. The future work may be,

- **Designing standard cell library for sub threshold devices**
- **Nano wire based sub threshold clock circuits**
- **Optical Interconnect based CDN**

References

[1] B. Calhoun, J. Ryan, S. Khanna, M. Putic, J. Lach, "Flexible Circuits and Architectures for Ultralow Power," Proceedings of the IEEE, Vol. 98, No. 2, Feb. 2010.

[2] B. C. Paul, A. Agarwal, K. Roy, "Low-Power Design Techniques for Scaled Technologies," Elsevier, integration, the VLSI journal 39, 64–89, 2006.

[3] H. Soleman, and K. Roy, "Ultra-low power Digital Sub-threshold Logic Circuits," in International Symposium on Low Power Electron. Design, pp.94-96, 1999.

[4] J. M. Rabaey, A. P. Chandrakasan, and B. Nikolic, " Digital Integrated Circuits-A Design Perspective, " 2nd Edition, Prentice Hall, New Jersey, USA, 2003.

[5] K. Roy and S.C. Prasad, "Low-Power CMOS VLSI Circuit Design," Wiley Inderscience Publications, New York, 2000.

[6] ITRS, International Technology Roadmap of Semiconductors, 2008, http://www.itrs.net

[7] H. Soeleman, K. Roy, B. C. Paul, "Robust Sub-threshold Logic for Ultra-Low Power Operation," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 9, No. 1, Feb. 2001.

[8] A. Wang, B. H. Calhoun, A. P. Chandrakasan, "Sub-Threshold Design for Ultra Low-Power Systems," First edition, Springer, New York, 2006.

[9] C. H. Kim and K. Roy, "Ultra-Low Power DLMS Adaptive Filter for Hearing Aid Applications," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 11, No. 6, pp. 352–357, Dec. 2003.

[10] J. Baker, "CMOS Circuit Design, Layout, and Simulation,"3rd_Edition, IEEE Press series on Microelectronics system, John Wiley & Sons, Inc., Publication, 2010.

[11] Y. Taur and T. H. Ning, "Fundamentals of Modern VLSI Devices," Second edition, Cambridge University Press, U.K., 2009.

[12] S. Hanson, M. Seok, D. Sylvester, D. Blaauw, "Nanometer device scaling in subthreshold logic and SRAM," IEEE Transactions on Electron Devices, Vol. 55, No. 1, pp. 175-185, Jan. 2008.

[13] N. Weste and D. Harris, "CMOS VLSI Design A Circuits and Systems Perspective," Fourth Edition Addison-Wesley, Pearson Education, 2010.

[14] B. Zhai, S. Hanson, D. Blaauw, D. Sylvester, "Analysis and Mitigation of Variability in Sub-threshold Design," ISLPED'05, Diego, California, USA, August-2005.

[15] R. Vaddi, S. Dasgupta and R. P. Agarwal, "Device and Circuit Co-Design Robustness Studies in the Sub threshold Logic for Ultralow-Power Applications for 32 nm CMOS," in IEEE Transactions on Electron Devices, Vol. 57, No. 3, pp: 654 – 664, March 2010.

[16] D. Bol, R. Ambroise, D. Flandre, J. Legat, "Interests and Limitations of Technology Scaling for Sub-threshold Logic," IEEE Transactions on VLSI Systems, Vol. 17, No.10, Sept. 2009.

[17] A. Tajalli and Y. Leblebici, "Design Trade-Offs in Ultra-Low Power Digital Nanoscale CMOS," IEEE Transactions on Circuits Systems - I, Vol. 58, No. 9, pp. 2189–2200, Sep. 2011.

[18] B. Datta and W. Burleson, "Temperature Effects on Energy Optimization in Sub-Threshold Circuit Design,"10th International Symposium on Quality Electronic Design.

[19] K. Roy, J. P. Kulkarni and M. E. Hwang, "Process-Tolerant Ultralow Voltage Digital Sub-threshold Design," IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF '08), pp. 42–45, Orlando, USA Jan. 2008.

[20] Y. Pu, J. P. De Gyvez, H. Corporaal and Y. Ha, "An Ultra-Low Energy Multi-Standard JPEG Co-Processor in 65 Nm CMOS with Sub/Near Threshold Supply Voltage," IEEE journal of solid state circuits, Vol. 45, No. 3, pp. 668 –680, 2010.

[21] B. Zhai, S. Pant, L. Nazhandali etal., "Energy-Efficient Sub-Threshold Processor Design," IEEE Transactions on VLSI systems, Vol. 17, No. 8, pp. 1127–1137, 2009.

[22] D. Markovoic, C. Wang, L. Alarcon, T. Liu, J. Rabaey, "Ultralow-Power Design in Near Threshold Region," Proceedings of the IEEE, Vol. 98, No. 2, Feb. 2010.

[23] K. Kim, Y. Kim, "A Novel Adaptive Design Methodology for Minimum Leakage Power Considering PVT Variations on Nanoscale VLSI Systems," IEEE Transactions on Very Large Scale Integrated (VLSI) Systems, Vol. 17, No. 4, April 2009.

[24] S. Hanson, B. Zhi, D. Biaauw, D. Sylvester, A. Bryant, X. Wang, "Energy Optimality and Variability in Sub-threshold Region," ISPLED'06, Tegernsee, Germany, 2006.

[25] B. C. Paul, A. Raychowdhuryand, K. Roy, "Device Optimization for Digital Sub-Threshold Logic operation," IEEE Transactions on Electron Devices, Vol. 52, No. 2, Feb. 2005.

[26] M. Nabavi, F. Ramezankhni, M. Shams, "Optimum PMOS - to -NMOS Width Ratio for Efficient Sub-threshold CMOS Circuits," IEEE Transactions on Electron Devices, Vol. 63, No. 3, March 2016.

[27] A. K. Kureshi, M. Hasan, "Analysis of CNT Bundle and its Comparison with Copper for FPGA Interconnect," International Journal of Applied Science, Engineering and Technology, 178–183, March 2009.

[28] G. T´ellez, M. Sarrafzadeh, "Minimal Buffer Insertion in Clock Trees with Skew and Slew Rate Constraints," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 16, No. 4, April 1997.

[29] S. D. Pable and M. Hasan, "Ultra-Low-Power Signalling Challenges for Sub-threshold Global Interconnects," Integration, the VLSI Journal, Elsevier.

[30] M. Seok, D. Blaauw, D. Sylvester, "Clock Network Design for Ultra-Low Power Applications,"ISLPED'10, Austin, Texas, USA, 18–20, Aug. 2010.

[31] F. Chen, A. Joshi, V. Stojanovic, and A. P. Chandrakasan, "Scaling and evaluation of carbon nanotube interconnects for VLSI applications," in Proc. International Conference on Nano-Net, Sep., 2007

[32] J. Kil, J. Gu, and C. H. Kim, "A High – Speed Variation – Tolerant Interconnect Technique for Sub-threshold Circuits using Capacitive Boosting," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 16, No.4, pp. 456-465, April 2008.

[33] S. D. Pable and M. Hasan, "High Speed Interconnect Through Device Optimization for Sub-threshold FPGA," Microelectronics Journal 42, 545–552, 2011.

[34] O. Jamal and A. Naeemi, "Ultra-Low-Power Single Wall Carbon Nanotube Interconnects for Sub-threshold Circuits," IEEE Transactions on Nanotechnology, Vol. 10, No. 1, pp. 99–101, Jan. 2011.

[35] O. Jamal and A. Naeemi, "Evolutionary and Revolutionary Interconnect Technologies for Performance Enhancement of Sub-threshold Circuits," IEEE Explore.

[36] N. Magen, A. Kolodny, Weiser, U. And N. Shamir, "Interconnect Power Dissipation in a Microprocessor," Proceedings of the International Workshop on System Level Interconnect Prediction, pp.7-13, 2004.

[37] V. Kaenel, "A High-Speed, Low-Power Clock generator for a Microprocessor Application," IEEE Journal of Solid-State Circuits, Vol. 33, No.11, Nov. 1998

[38] J. Tolbert, X. Zhao, S. K. Lim and S. Mukhopadhyay, "Slew-Aware Clock Tree Design for Reliable Sub-threshold Circuits," International Symposium of Low Power Electronics and Design, August, pp. 15-20, 2009.

[39] J. Jalil, M. Reaz, and M. Ali, "CMOS differential ring oscillators: Review of the performance of CMOS ROs in communication systems," IEEE Microwave Magazine, Vol. 14, No. 5, pp. 97–109, July 2013.

[40] P. Kamalinejad, K. Keikhosravy, R. Molavi, S. Mirabbasi, and V. Leung, "An Ultra-Low-Power CMOS Voltage-Controlled Ring Oscillator for Passive RFID

Tags," International New Circuits and Systems Conference, IEEE, pp. 456-459, 2014.

[41] S. K. Saw and V. Nath, "An Ultra Low Power and Low Phase Noise Current starved CMOS VCO for Wireless Application," International Conference on Industrial Instrumentation and Control (ICIC), 2015.

[42] Y. I. Ismail, E. G. Friedman," Effects of inductance on the propagation delay and repeater insertion in VLSI circuits," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 8, No. 2 , pp. 195–206, 2000.

[43] C. Sitik, S. Lerner and B. Taskin, "Timing Characterization of Clock Buffers," IEEE 32nd International Conference on Computer Design (ICCD) , 2014.

[44] P. Zarkesh-Ha, T. Mule, and J. Meindl, "Characterization and Modeling of Clock Skew with Process Variations", Proceedings of IEEE Custom Integrated Circuits Conference, 1999.

[45] R. Barnett and Jin Liu, "A 0.8V 1.52MHz MSVC Relaxation Oscillator with Inverted Mirror Feedback Reference for UHF RFID," in Custom Integrated Circuits Conference, pp. 769-772, 2006.

[46] P. Rout, D. Acharya and G. Panda, "A Multiobjective Optimization Based Fast and Robust Design Methodology for Low Power and Low Phase Noise Current Starved VCO," IEEE Transactions on Semiconductor Manufacturing, Vol. 27, No. 1, Feb. 2014.

[47] S. Lee, J. Hsieh, "Analysis and Implementation of a 0.9-V Voltage-Controlled Oscillator with Low Phase Noise and Low Power Dissipation," IEEE Transactions on Circuits and Systems –II, Express Briefs, Vol. 55, No. 7, July 2008.

[48] T. Lee, Y- Kim, J. Sim, J. Park and L. Kim, "A 5-Gb/s 2.67-mW/Gb/s Digital Clock and Data Recovery with Hybrid Dithering using a Time-Dithered Delta–Sigma modulator," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015.

[49] K. Ryu, J. Jung, D. Jung, J. Kim, S. Jung, "High Speed, Low Power and Highly Reliable Frequency Multiplier for DLL Based Clock Generator," IEEE Transactions on Very Large Scale (VLSI) Systems, 2015.

[50] F. Marraccini, G. DeVita, S. DiPascoli, G. Iannaccone, "Low-Voltage Nanopower Clock Generator for RFID Applications," Microelectronics Journal 39, 1736– 1739, 2008.

[51] S. Kumar Saw, Vijaynath, "A Low Power Low Noise Current Starved CMOS VCO for PLL," International Conference on Computing, Communication and Automation, ICCCA-2015.

[52] P. Khurana, R. Kumar, "Performance Analysis of CMOS Based Ring VCO's," International Journal of Engineering, Technology, Management and Applied Sciences, Vol. 2, Issue 4, ISSN 2349-4776, Sept. 2014.

[53] P. Tsai, T. Huang, "Integration of Current Reused VCO and Frequency Tripler for 24 GHz Low Power Phase-Locked Loop Applications," IEEE Transactions on Circuits and Systems, Vol. 59, No. 4, April 2012.

[54] W. Rim, W. Choi, J. Park, "Adaptive Clock Generation Technique for Variation-Aware Sub-threshold Logics," IEEE Transactions on Circuits & Systems-II, Vol. 59, No. 9, Sept. 2012.

[55] R. D. Jorgenson, L. Sorensen, D. Leet, M. S. Hagedorn, D. R. Lamb, T. H. Friddell, and W. P. Snapp, "Ultralow-Power Operation in Sub-threshold Regimes Applying Clockless Logic," Proc. IEEE, Vol. 98, No. 2, pp. 299–314, Feb. 2010.

[56] B. Ghavami, H. Pedram, and M. Najibi, "An EDA Tool for Implementation of Low Power and Secure Crypto-Chips," Comput. Electr. Eng., Vol. 35, No. 2, pp. 244–257, March 2009.

[57] S. Farzeen, G. Ren, and C. Chen, "An Ultra-Low Power Ring Oscillator for Passive UHF RFID Transponders," IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), pp. 558–561, August 2010.

[58] S. Park, C. Min and S. Cho, "A 95nw Ring Oscillator-Based Temperature Sensor for RFID Tags In 0.13µm CMOS," IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1153–1156, May 2009.

[59] Y. Wang, J. LIU, L. XIE, G. WEN, "An Ultra-Low-Power Oscillator with Temperature and Process Compensation for UHF RFID Transponder," Radio Engineering, Vol. 22, No. 2, June 2013.

[60] X. Zhang, A. B. Apsel, " A Low Variation GHz Ring Oscillator with Addition Baed Current Source," Proceedings of ESSCIRC IEEE, 2009.

[61] C. Zhang, M. Lin, M. Syrzycki, "Process Variation Compensated Voltage Controlled Ring Oscillator with Subtractor- Based Voltage Controlled Current Source," CCECE, IEEE, 2011.

[62] Y. Ho, K. Li, and S. Wang, "A 0.3 V Low- Power Temperature Insensitive Ring Oscillator in 90nm CMOS Process", International Symposium on VLSI Design, Automation, and Test (VLSI-DAT), IEEE, 2013.

[63] K. Lasanen, E.R. Ruotsalainen, J. Kostamovaara, "A 1-V, Self Adjusting, 5-MHz CMOS RC-Oscillator," in Proceeding of ISCAS, Scottsdale, USA, vol. IV, pp. 377-380, 2002.

[64] F. Bala, T. Nandy, "Programmable High Frequency RC Oscillator," International Conference on VLSI Design, pp. 511-515, 2005.

[65] G. D Vita, F. Marraccini and G. Iannaccone "Low-Voltage Low-Power CMOS Oscillator with Low Temperature and Process Sensitivity," in Proceeding of International Symposium on Circuits and Systems. IEEE, pp. 2152-2155, 2007.

[66] S. Kaya and A. Kulkarni, "A Novel Voltage Controlled Ring Oscillator Based on Nanoscale DG-MOSFETs," in International Conference on Microelectronics, pp.417-420, 2008.

[67] V. Yanambaka, S. Mohanty, E. Ougianos, D. Ghai, G. Ghai, "Process Variation Analysis and Optimization of FinFET Based VCO," IEEE Transaction on Semiconductor Manufacturing, Vol. 30, No. 2, 2017.

[68] D. Ghai, S. P. Mohanty and G. Thakral, "Double Gate FinFET Based Mixed-

Signal Design: A VCO Case Study," International Midwest Symposium on Circuits and Systems (MWSCAS), IEEE, 2013.

[69] S. Saxena, M. Srikanth, S. Jawale and R. Sakthivel, " Efficient VCO using FinFET," in Indian Journal of Science and Technology, Vol. 8(S2), 262–270, 2015.

[70] X. Liu, C. Lee, J. Han, C. Zhou ,"Carbon Nanotube Feld-Effect Inverters," Appl. Phys. Lett., 79, pp. 3329–3331, 2001.

[71] A. Javey, Q. Wang, A. Ural, Y. Li, H. Dai, "Carbon Nanotube Transistor Arrays for Multi Stage Complementary Logic and Ring Oscillators," Nano Lett.,2, pp: 929-932, 2002.

[72] C. Wang, A. Badmaev, A. Jooyaie, M. Bao, K. L. Wang, G. Kosmas and C. Zho, "Radio Frequency and Linearity Performance of Transistors using High-Purity Semiconducting Carbon Nanotubes," ACS Nano, 5, pp. 4169–4176, 2011.

[73] S. I. Sayed, M. M. Abutaleb and Z. B. Nossair, "Performance Optimization of Logic Circuits Based on Hybrid CMOS and CNFET Design," International Journal of Recent Technology and Engineering, Vol. 1, No. 6, pp. 1–4, 2013.

[74] D. Akinwande, S. Yasuda, B. Paul, S. Fujita, G. Close and H-S. P. Wong, "Monolithic Integration of CMOS VLSI and Carbon Nanotubes for Hybrid Nanotechnology Applications," in IEEE Transactions on Nanotechnology, Vol. 7, No. 5, pp. 636–639, 2008.

[75] K. K. Kim, Y. B. Kim , K. Choi, "Hybrid CMOS and CNFET Power Gating in Ultralow Voltage Design," in IEEE Transactions on Nanotechnology, 10(6), 2011.

[76] P. Zhang, Y. Yang, T. Pei, C. Qiu, L. Ding, S. Liang, Z. Zhang and L. Peng, "Transient Response of Carbon Nanotube Integrated Circuits," Nano Research, Vol. 8, No. 3, pp. 1005–1016, 2015.

[77] S. I. Sayed, M. M. Abutaleb, Z. B. Nossair, "Optimization of CNFET Parameters for High Performance Digital Circuits," in Advances in Materials Science and Engineering Volume, Article ID 6303725, 2016.

[78] H. Nan, K. K. Kim, K. Choi, "Novel CNFET SRAM Cell Design Operating in Sub-Threshold Region using Back-Gate Biasing," in IEEE International Conference on Electro/Information Technology, 2010.

[79] M. Moradinasab, M. Fathipour, "Stable, Low Power and High Performance SRAM Based on CNFET," 10th International Conference on Ultimate Integration of Silicon, 2009.

[80] E. G. Friedman, "Clock Distribution Networks in Synchronous Digital Integrated Circuits," Proc. of IEEE, 89(5):665–692, May 2001.

[81] J. Reuben, M. Zackriya, V. Harish, M. Shoaib, "A Buffer Placement Algorithm to Overcome Short-Circuit Power Dissipation in Mesh Based Clock Distribution Network," Engineering Science and Technology, an International Journal 18, 135-140, 2015.

[82] A. Rajaram, H. Jiang and R. Mahapatra, "Reducing Clock Skew Variability via Cross links," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 25, No. 6.

[83] M. Dave, M. Jain, M. Baghini, D. Sharma, "A Variant Tolerant Current Mode Signalling Scheme for On Chip Interconnects," IEEE Transactions on Very Large Scale (VLSI) Systems, Vol. 21, No. 2, Feb. 2013.

[84] R. Islam, M. Gauthas, "Low Power Clock Distribution Using A Current Pulsed Clocked Flip-Flop," IEEE Transactions on Circuits and Systems-I Regular Papers, Vol. 62, No. 4, April 2015.

[85] A. Abdelhadi, R. Ginosar, A. Kolodny, E. Friedman, "Timing Driven Variation Aware Synthesis of Hybrid Mesh / Tree Clock Distribution Networks," Integration, the VLSI journal 46, 382–391, 2013.

[86] L. Gaioni, F. DeCanio, M. Manghisoni, L. Ratti, V. Re, G. Traversi, "Design and Test of Clock Distribution Circuits for the Macro Pixel ASIC," Nuclear Instruments and Methods in Physics Research, Elsevier, 2015.

[87] V. Tenace, S. Miryala, A. Calimera, A. Macii, E. Macii, M. Poncino, "Row Based Body Bias Assignment for Dynamic Thermal Clock-Skew Compensation," Microelectronics Journal 45, 530-538, 2014.

[88] W. K. Loo, K. S. Tan, & Y. K. Teh, "A Study and Design of CMOS H-Tree Clock Distribution Network in System-on-Chip," 8th International Conference on ASIC, IEEE, 2009.

[89] S. Choudhary, & S. Qureshi, "Design, Modelling and Simulation of H tree Clock Distribution Network," Australian Journal of Electrical & Electronics Engineering, Vol. 7, No. 3, pp. 257-264, 2010.

[90] Berkeley Predictive Technology Model, UC Berkeley Device Group. [Online]. Available: /http//www.eas.asu.edu/ptm

[91] X. C. Li, J. F. Mao, H. F. Huang, Y. Liu, "Global Interconnect Width and Spacing Optimization for Latency, Bandwidth and Power Optimization," IEEE Transaction on Electron Devices, Vol. 52, No. 10, pp.-2272-2279, 2005.

[92] R. H. Reuss, and M. Fritze, "Introduction to Special Issue on Circuit Technology for ULP," in Proc. IEEE, Vol. 98, Issue No. 2, pp. 139–143, 2010.

[93] D. Nirmal, P. Vijayakumar, P. Samuel, B. Jebalin, N. Mohankumar, "Subthreshold Analysis of Nanoscale Finfets for Ultra Low Power Application Using High – K Dielectric Materials," International Journal of Electronics, 100:6,803-817, 2012.

[94] X. Wu, F. Wang and Y. Xie, "Analysis of Sub threshold FinFET Circuits for Ultra Low Power Design," SOC Conference, IEEE, 2006.

[95] A. Dadoria, K. Khare, T. Gupta, R. Singh, "Ultra Low FinFET Based Domino Circuits," International Journal of Electronics, 2017.

[96] S. Spedo, C. Fiegna, "Comparison of Symmetric and Asymmetric Double Gate Mosfets-Tunneling Current and Hot Electrons," Semiconductor Device

Research Symposium, IEEE, 2001.

[97] Q. Chen and J. D. Meindl, "A Comparative Study of Threshold Variations in Symmetric and Asymmetric Undoped Double-Gate MOSFETS," in proceedings of International SOI Conference, pp-30-31, 2002.

[98] R. Cakici and K. Roy, "Analysis of Options in Double-Gate MOS Technology: A Circuit Perspective," IEEE Transactions on Electron Devices Vol. 54, No.12, 2007.

[99] K. Kim, J. Fossum, "Double-Gate CMOS: Symmetrical or Asymmetrical Gate Devices," IEEE Transaction on Electron Devices, Vol. 48. No. 2, pp-294-299, 2001.

[100] R. Vaddi, S. Dasgupta, R. Agarwal, "Robustness Comparison of DG Finfets with Symmetric, Asymmetric, Tied and Independent Gate Options with Circuit Co-Design for Ultra Low Power Sub threshold Logic," Microelectronics journal, Vol. 41, No. 4, pp. 195-211, 2010.

[101] T. Dürkop, S. A. Getty, E. Cobas, and M. S. Fuhrer, "Extraordinary Mobility in Semiconducting Carbon Nanotubes," in Nano Letters, 4(1), pp 35–39, 2004.

[102] A. Javey, J. Guo, Q. Wang, M. Lundstrom and H. Dai, "Ballistic Carbon Nanotube Field-Effect Transistors," in Nature, 424(6949), pages 654–657, 2003.

[103] A. Javey, Q. Wang, W. Kim, and H. Dai, "Advancements in Complementary Carbon Nanotube Field-Effect Transistor," in Proc. IEEE Int. Electron Devices Meeting, pp. 31.2.1–31.2.4, 2003.

[104] J. Deng and H. Wong, "A Compact Spice Model for Carbon-Nanotube Field-Effect Transistors Including Non-idealities and its Application-Part I-Model of Intrinsic Channel Region," IEEE Trans. Electron. Devices, vol. 54, no. 12, pp. 3186–3194, 2007.

[105] A. Rahman, J. Guo, S. Datta and M. S. Lundstrom, "Theory of Ballistic Nano transistors," IEEE Trans. Electron Devices, Vol. 50, No. 10, pp. 1853–1864, Sep. 2003.

[106] A. Akturk, G. Pennington, N. Goldsman and A. Wickenden, "Electron Transport and Velocity Oscillations in a Carbon Nanotube," IEEE Trans. Nanotechnol., Vol. 6, No. 4, pp. 469–474, 2007.

[107] H. Hashempour and F. Lombardi, "Device Model for Ballistic CNFETs using the First Conducting Band," IEEE Design Test Comput., Vol. 25, No. 2, pp. 178–186, 2008.

[108] Y. Lin, J. Appenzeller, J. Knoch and P. Avouris, "High Performance Carbon Nanotube Field-Effect Transistor with Tunable Polarities," IEEE Trans. Nanotechnol., Vol. 4, No. 5, pp. 481–489, Sep. 2005.

[109] N. Patil, A. Lin, J. Zhang, H. Wong and S. Mitra, "Digital VLSI Logic Technology using Carbon Nanotube FETs: Frequently Asked Questions," in Proc. IEEE Design Autom. Conf., pp. 304–309, 2009.

[110] A. D. Franklin, M. Luisier, S. J. Han, G. Tulevski, C. M. Breslin, L. Gignac, S. Mark, Lundstrom, and W. Haensch, "Sub-10 nm Carbon Nanotube Transistor," Nano Lett., 12 (2), pp 758–762, 2012.

[111] L. Ding, S. Liang, T. Pei, Z. Zhang, S. Wang, W. Zhou, J. Liu and L. M. Peng, "Carbon Nanotube Based Ultra-Low Voltage Integrated Circuits: Scaling Down to 0.4 V," Applied Physics Letters, 2012.

[112] M. S. Dresselhaus, G. Dresselhaus and Ph. Avouris, "Carbon Nanotubes: Synthesis, Structure Properties and Applications," Springer-Verlag, Berlin, 2001.

[113] H. S. P. Wong, J. Deng, Arash, Hazeghi, T. Krishnamohan, G. C. Wan, "Carbon Nanotubes Transistor Circuits-Models and Tools for Design and Performance Optimization," in IEEE/ACM International Conference on Computer Aided Design, pp.651-654, 2006.

[114] F. A. Usmani and M. Hasan, "Carbon Nanotube Field Effect Transistors for High Performance Analog Applications: An Optimum Design Approach," Microelectronics Journal, Vol. 41, No. 7, pp. 395–402, 2010.

[115] J. Kim and K. Roy, "Double Gate-MOSFET Sub threshold Circuit for Ultra Low Power Applications," IEEE Transactions on Electron Devices, Vol. 51, No. 9, pp. 1468-1474, 2004.

[116] Stanford University Carbon Nanotube Field Effect Transistors (CNFET) HSPICE Model [online] Available: https://nano.stanford.edu/stanford-cnfet-model-hspice.

[117] R. Chaturvedi and J. Hu, "Buffered Clock Tree for High Quality IC Design," International Symposium on Signals, Circuits and Systems, Proceedings, SCS, IEEE, 2004.

[118] C. Sitik, E. Salman, L. Filippini, S. J. Yoon and B. Taskin, "Finfet Based Low Swing Clocking," ACM Journal on Emerging technologies in Computing Systems,Vol.12, No. 2, 2015.

[119] A. Olmos, "A Temperature Compensated Fully trimmable on Chip IC Oscillator," Integrated Circuit and System design, 181–186, 2003.

[120] W. Yang, C. Wang and I. Chuo, "A Robust Oscillator for Embedded System without External Crystal," International Journal on Applications Math. Inf, Sciences, 9(11).

[121] N. Gargouri, Z. Sakka, D. Issa, A. Kacchouri and M. Same, "A 4 GHz Temperature Compensated CMOS Ring Oscillator for Impulse Radio UWB," International Conference on Sciences of Electronics, Technologies of Information and Telecommunications, 2017.

[122] J. Colinge, "Novel Gate Concept of MOS Devices," in Proceeding of the Solid-State Device Research Conference, 2004.

[123] R. A. Walunj, S. D. Pable, G. K. Kharate, "Ultra Low Power DG FinFET based Voltage Controlled Oscillator Circuits," International Journal of Electronics, 106:1, 134-159, 2019.

[124] D. Fathi, B. B. Mohammadi, "Millimeter Wave Ring Oscillator using Carbon Nano-Tube Field Effect Transistor in 150 GHz and Beyond," Circuits and Systems, Vol. 4 No. 2, 2013.

Research Publications

Journal

1. R. A. Walunj, S. D. Pable, G. K. Kharate, "Challenges in Designing Ultra-Low Power VCO," Journal of Active and Passive Electronic Devices, in Press, 2017.

2. R. A. Walunj, S. D. Pable, G. K. Kharate, " Design of Thermally Aware Ultra Low Power Clock Generator for Moderate Speed VLSI Chip Applications," in Australian Journal of Electrical and Electronics Engineering," Taylor and Francis, 15:1-2, 9-20.

3. R. A. Walunj, S. D. Pable, G. K. Kharate, "Ultra Low Power DG FinFET Based Voltage Controlled Oscillator Circuits," in International Journal of Electronics, Taylor and Francis, 106:1, 134-159.

4. R. A. Walunj, S. D. Pable, G. K. Kharate, "Design Considerations and Optimization of Clock Circuit for Ultra-Low Power Sub threshold Applications," in Australian Journal of Electrical & Electronics Engineering, Taylor and Francis, 15:3, 98-117.

5. R. A. Walunj, S. D. Pable, G. K. Kharate, "Design of Slew Aware Clock Distribution Network for Ultra Low Power Sub threshold Applications," in Journal of VLSI Design Tools and Technology, 9(1), 22–37, 2019.

6. R. A. Walunj, S. D. Pable, G. K. Kharate, "Performance Optimization of CNFET Based Voltage Controlled Oscillator Circuit in Sub threshold Regime," in Microelectronics Journal, Elsevier (Under Revision).

International Conference

1. R. A. Walunj, S. D. Pable, G. K. Kharate, "Impact of Interconnect Variation on Ultra Low Power Clock System," in ICCCC 2017, Matoshri College of Engineering & Research Centre, Nasik.

2. R. A. Walunj, S. D. Pable, G. K. Kharate, "Design of Robust Ultra-Low Power CMOS Voltage Controlled Ring Oscillator with Enhanced Performance," in IEEE "International Conference on Advances in Communication and Computing Technology (ICACCT), 2018.

3. R. A. Walunj, S. D. Pable, G. K. Kharate, "Performance Analysis of Voltage Controlled Oscillator with 32nm MOSFET, DG-FinFET and CNFET," Accepted in International Conference on Industrial and Information Systems (ICIIS 2018), IIT Ropar (Accepted).